

Paging Encoders

MODEN 100

MODEN 36

Alert Central





INSTRUCTION MANUAL REVISION FOR

68P81012C20-0
PAGING ENCODERS
REPLACE PAGES 17 & 18 WITH THESE PAGES 17 & 18

A three-wire power system or appropriate grounded plug adapter must be used.

(b) DC Power Source

If a dc power source is to be used, the paging encoder requires a 12- to 18-volt dc power source with a continuous current drain of 40 milliamperes minimum and 250 milliamperes maximum. The minimum current drain is measured by entering a paging call code into the keyboard: 11 for "Moden" 100 and 36 paging encoders. For Alert Central paging encoder, a one is entered, but the measurement is taken after the automatic page mode terminates. The maximum current drain is measured by entering a different paging call code into the keyboard (88 for "Moden" 100, 00 for "Moden" 36, and 0 (red pushbutton) for Alert Central); and then the keyboard page pushbutton is depressed. The maximum current drain measurement is taken during the paging mode.

The paging encoder does not include fuse protection for the dc input power source; therefore, cable TKN6323 is recommended because it has a built-in fuse. Connection of the dc power source must be made to main circuit board screw terminals DC+ and GND.

NOTE

Observe polarity when connecting a power source to the paging encoder. If the polarity is reversed, the logic circuitry will be inoperative.

(2) Interference

As with any complex electronic facility, the performance of this paging encoder may be degraded by spurious signals received from outside sources. Minimize the possibility of interference by selecting a paging encoder location away from generators of electrical noise such as large motors, switchgear, welding equipment, etc.

The digital logic circuitry used in the paging encoder, although immune to most low-level interference, is particularly susceptible to discharges of static electricity. These discharges, which often reach high potentials, introduce errors and may cause erratic operation. Nonconductive household carpeting provides an excellent medium for the generation of static potentials and this type of floor covering is NOT recommended for use at the paging encoder site. It is recommended that conductive carpeting or tile, manufactured especially for electronic installations, be used in the paging encoder site. If a conductive floor

covering is not used, the area around the paging encoder must be sprayed with an antistatic compound at least once a week during periods of low humidity. A suitable chemical is supplied in spray cans under the brand name "Static-Stop," manufactured by Barco Chemical Products, Chicago, Illinois. Other equivalent products are available and these should serve just as well. However, be sure that the product will not damage the floor covering nor the paging encoder housing.

4. PREOPERATIONAL CHECK

a. "Moden" 100 and "Moden" 36 Paging Encoder

- (1) Plug the paging encoder into an ac power source and set the AC-OFF-DC switch to the AC position. The digit display should be "00."
- (2) Enter a two-digit number into the paging encoder using the numbered keyboard pushbuttons. Note that the numbers are displayed from right to left as they are entered.
- (3) Depress the keyboard page (P) pushbutton and note that the PAGE indicator lamp begins to glow.
- (4) The PAGE indicator lamp stops glowing after the paging mode is automatically terminated. On the "Moden" 100 paging encoder, note that the TALK indicator lamp begins to glow. The TALK lamp continues to glow until the unit is switched off. (When either JUl or 2 is cut, the TALK light will illuminate during the talk cycle for eight to ten seconds.
- (5) Set the AC-OFF-DC switch to the OFF position and unplug the paging encoder from the power source.

b. Alert Central Paging Encoder

- (1) Plug the paging encoder into an ac power source and set the AC-OFF-DC switch to the AC position. The digit display should be "0."
- (2) Depress a numbered keyboard pushbutton. Note that the number depressed is displayed and the PAGE indicator lamp begins to glow. Approximately four to six seconds later the PAGE lamp stops glowing.
- (3) Set the AC-OFF-DC switch to the OFF position and unplug the paging encoder from the power source.

5. MOUNTING

The paging encoder can be placed on any flat, level, surface such as a desk top which provides the operator full visibility of all keyboard pushbuttons and indicators.

6. OPTIONAL JUMPER AND TONE TIMING RESISTOR CONFIGURATIONS

Optional jumper and tone timing resistor configurations on the main circuit board are described here. Not all jumpers are covered in this description; the schematic diagram shows jumper differences between models of the paging encoders described in this manual.

Remove the top cover of the paging encoder housing as described in "Preliminary Equipment Checks" of this section. Refer to Figure 3 for jumper locations.

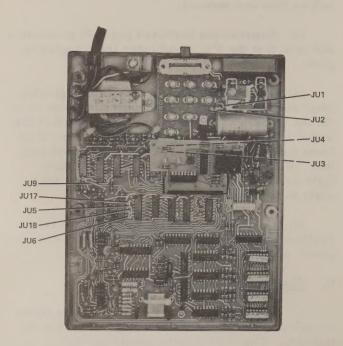


Figure 3. Optional Jumper Locations

a. Optional Jumpers

(1) Jumper JU1

Jumper JUl is used for carrier squelch systems and cut out for PL squelch systems.

(2) Jumper JU2

Jumper JU2 is used for PL "Mocom," PL "Maxar," and PL "Compa-Station" base stations and cut out for all other Motorola base stations.

(3) Jumper JU3

Jumper JU3 is used for all except PL "Mocom" and PL "Maxar" base stations where it is cut out.

(4) Jumper JU4

Jumper JU4 is used for PL "Maxar" base stations and cut out for all other base stations.

(5) Jumpers JU5 and JU6

Jumpers JU5 and JU6 are used for all "Moden" 100 and "Moden" 36 Paging Encoders and also for Alert Central paging encoders with the fixed tone A option. They are cut out for standard Alert Central Paging Encoders with the fixed tone B. These two jumpers are used in conjunction with jumpers JU17 and JU18.

(6) Jumper JU9

Jumper JU9 is used for all Alert Central paging encoders and cut out for all other "Moden" Paging Encoders described in the manual. When jumper JU9 is in, pin 8 of keyboard plug Pl (black wire) is tied back and not connected to plug Pl.

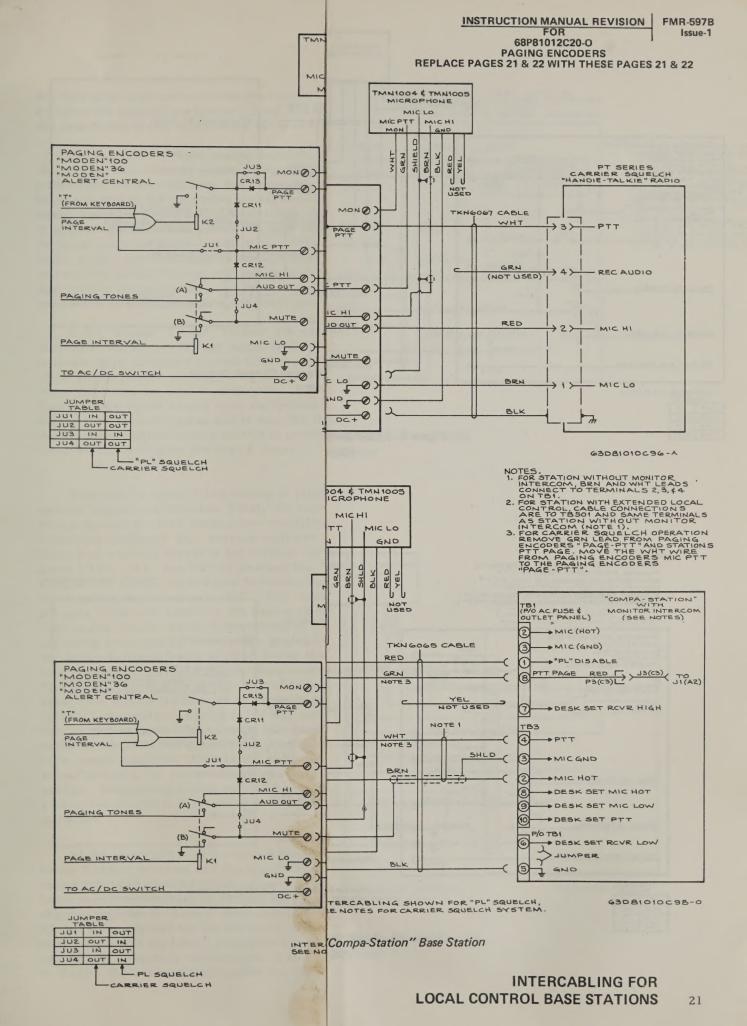
(7) Jumpers JU17 and JU18

Jumpers JU17 and JU18 are used for standard Alert Central paging encoders with the fixed tone B and are cut out of all other "Moden" Paging Encoders described in this manual. These two jumpers are used in conjunction with jumpers JU5 and JU6.

b. Tone Timing Resistors

Depending upon the order, the paging encoder is shipped from the factory with the tone timing set for tone-only or tone-and-voice operation. Table 22 lists resistors and values that are changed according to the timing desired.

The times shown in Table 22 are the times required by the paging receiver. In tone remote control systems, the RC time constant should account for the 200 milliseconds that tone A is muted while the transmitter turn-on tones are being sent.



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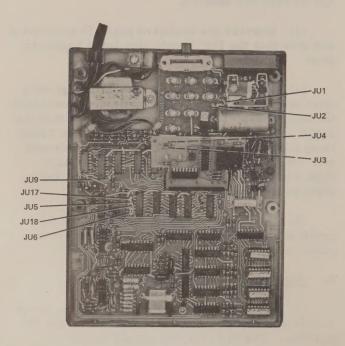


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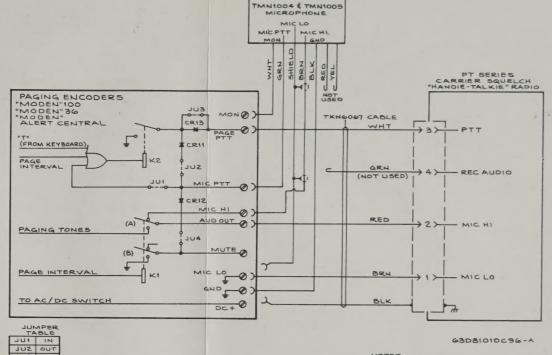
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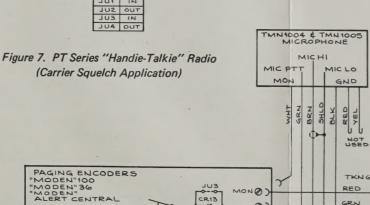
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REPLACE PAGES 21 & 22 WITH THESE PAGES 21 & 22





JU3 CR13

CP44

JUZ

K2

(B)

L PL SQUELCH -CARRIER SQUELCH

(FROM KEYBOARD)

PAGING TONES

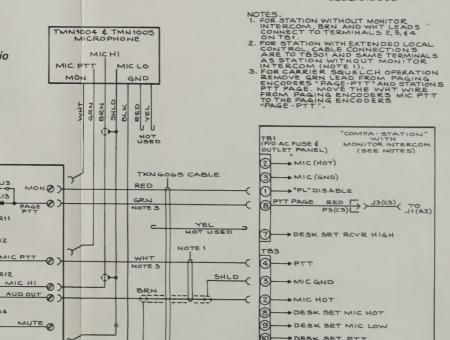
PAGE INTERVAL

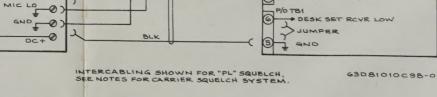
TUO NI PUL

JU3 IN IN JU4 OUT OUT

TO AC / DC SWITCH

PAGE







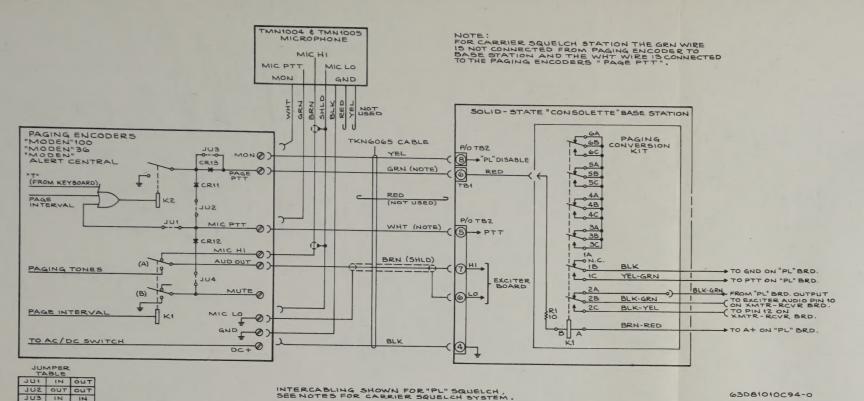
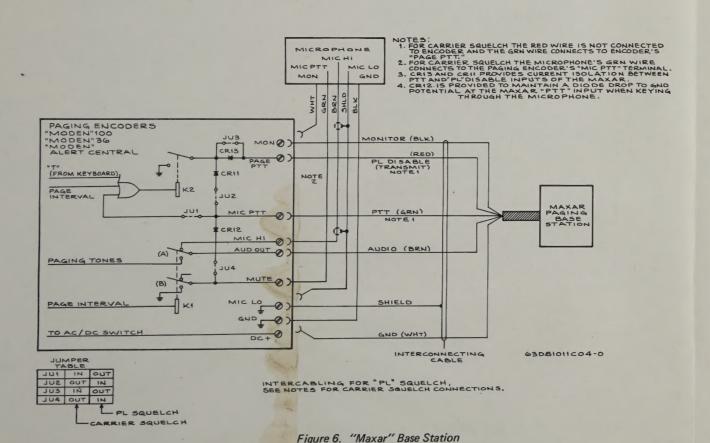
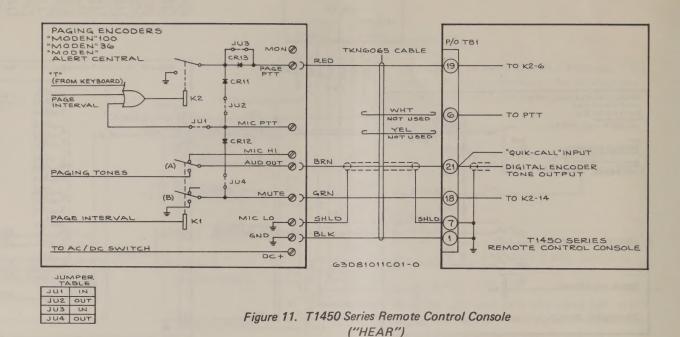
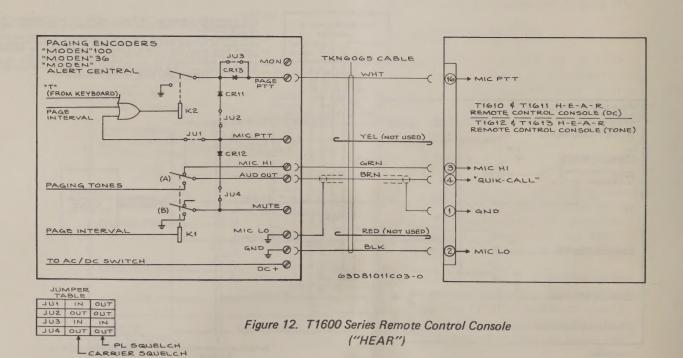


Figure 5. "Consolette" Base Station



"PL" SQUELCH





the circuitry required to enable the transmitter, initiates the appropriate timing cycles, and enables the generation of the appropriate encoder tones.

For the Alert Central paging encoder, after the paging call code or group call code (red pushbutton) is entered into the keyboard, the keyboard strobe load/transfer pulse, simultaneously, loads the paging call code digit into register B and, via jumper JU9, pulses the page input to keyboard page debounce circuit U7A. This automatic paging function initiates the circuitry required to enable the transmitter, initiates the appropriate timing cycles, and enables the generation of the appropriate encoder tones.

In the ''Moden'' 36 and ''Moden'' 100 paging encoders, the keyboard page signal is fed through keyboard page debounce circuit U7A to produce a clean strobe to prevent triggering the tone A timer more than once for each timing cycle. The Alert Central page signal comes from the keyboard strobe load/transfer pulse and is also fed through the keyboard page debounce circuit to produce a clean strobe to trigger the tone A timer.

When tone A timer U14A timing is initiated, several stages are enabled. First, the tone A timer enables the tone burst select multiplexer to sample keyboard data storage register A. The same enabling signal is fed through OR gates U13B, U8A, and U8B to produce the synthesizer enable input signal to divide-by-8 U16B and paging relay gate U1C. The output of OR gate U13B also produces the keyboard disable input signal which disables the keyboard from accepting more paging codes while paging. The divide-by-8 circuit being enabled routes the tone A paging tone to the paging relay contact. The synthesizer enable at the input of paging relay gate UIC is fed through to energize paging relay Kl, to energize keying relay K2, and to turn on paging lamp CR9. Energizing paging relay Kl connects the synthesizer paging tones from output amplifier U31B to the audio output screw terminal for transmission by a base station. Energizing keying relay K2 provides a switched ground to the base station for keying purposes.

At the termination of the tone A timer, tone B timer U14B is initiated and the signal level to U9 select inputs is changed which causes the tone burst select multiplexer to sample keyboard data storage register B. Tone B timer maintains relays K1 and K2 energized for its duration, allowing the transmission of the tone B paging tone from the paging tone frequency synthesizer. It also continues to disable the keyboard and enable the synthesizer.

For the "Moden" 36 and the Alert Central paging encoders, if a voice message is to be sent, the keyboard talk pushbutton must be depressed before the page lamp goes out (gaptime terminated). By depressing the keyboard talk pushbutton, keying relay K2 is kept energized through keying relay gate U11B and U12A while the paging relay and lamp are de-energized when the gap timer terminates. A voice message can be given as long as the keyboard talk pushbutton is depressed.

When the "Moden" 100 paging encoder tone timer B terminates, gates U13B, U8A, and U8B remove the synthesizer enable signal from the divide-by-8 input so that paging tones will no longer be generated. It also removes the keyboard disable signal to enable the keyboard to accept a new paging code. The enabling pulse to the input of paging relay gate U1C is removed when the tone B timer terminates, but at the same time, when gap timer U23A is initiated, another enabling pulse is routed to the input of paging relay gate U1C to maintain the paging and keying relays and the paging LED energized.

The gap timer provides a gap or space between the paging tones and the voice message to allow the paging receiver to enable its audio circuitry to receive a voice message after receiving tone B.

At the end of the gap timer timing cycle, relay K1 is de-energized, paging lamp CR9 goes out, the audio output switches from the paging tone input to the microphone audio input, talk timer U23B is initiated to maintain keying relay K2 in its energized condition, and talk lamp CR10 begins to glow. The talk time is nominally 10 seconds for sending a voice message.

If no voice message is sent, another paging code can be entered into the keyboard data storage registers and another page initiated by depressing the page pushbutton. This resets the talk timer and starts the tone timing over again.

The talk timer timing cycle can be shortened by momentarily depressing ("flashing") the keyboard talk pushbutton or the microphone push-totalk paddle.

A voice message, not preceded by a paging tone, can be transmitted by depressing the keyboard talk pushbutton or microphone push-to-talk paddle. This energizes keying relay K2 through keying relay enable gate U12A which will key the base station transmitter. Relay K1 is in the de-energized state and therefore, microphone audio is routed through to the base station. The talk lamp is energized through talk lamp enable gate U13A.

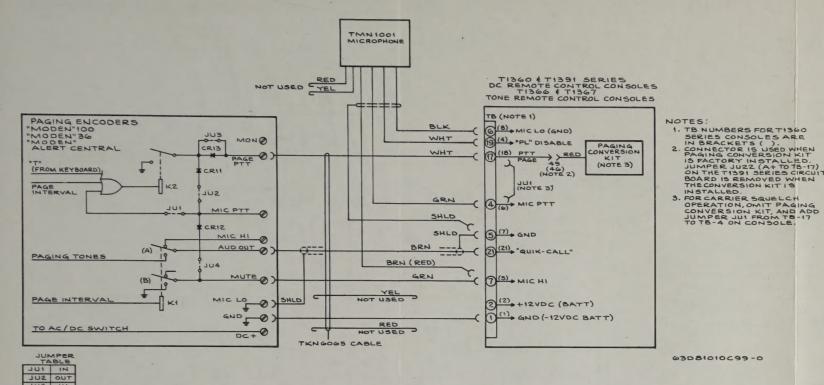
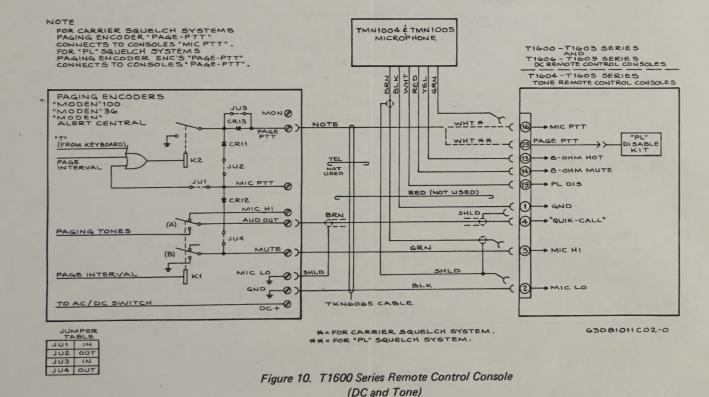


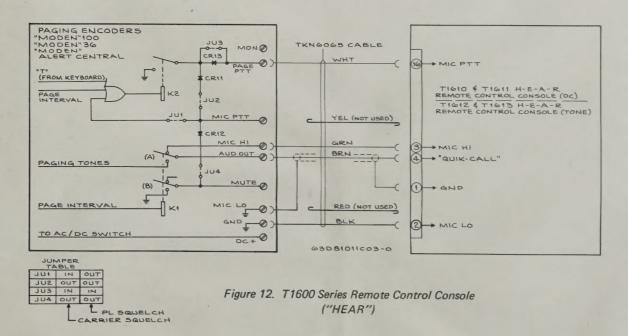
Figure 9. T1300 Series Remote Control Console (DC and Tone)



PAGING ENCODERS
"MODEN" 100
"MODEN" 36
"MODEN"
ALERT CENTRAL JU3 CR13 MONO TKNG065 CABLE RED PAGE 0 - TO K2-6 CRII (FROM KEYBOARD) MIC PTT YEL -CR12 MIC HI - "QUIK-CALL" INPUT AUD OUT PAGING TONES MUTE 0 (B) PAGE INTERVA WIC TO CND -0 T1450 SERIES REMOTE CONTROL CONSOLE TO AC/DC SWITCH DC+0 63D81011C01-0 JUMPER TABLE JUI IN JU2 OUT JU3 IN

Figure 11. T1450 Series Remote Control Console

("HEAR")



68P81012C20-O
PAGING ENCODERS
REPLACE PAGES 35 & 36 WITH THESE PAGES 35 & 36

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MAINTENANCE

1. INTRODUCTION

This section describes recommended repair procedures, special precautions regarding maintenance, recommended test equipment, and system troubleshooting techniques. Each of these topics provides information vital to the successful operation and maintenance of the "Moden" Series Paging Encoders described in this manual.

2. PREVENTIVE MAINTENANCE

a. Visual Inspection

Check that external surfaces of the equipment are clean, that connecting cables and wires are not damaged, and that connections are firm. A detailed inspection of the interior electronic circuits is not needed or desired.

b. Cleaning

Periodically clean smudges and grime from the exterior of the housing. Use a soft, nonabrasive cloth <u>moistened</u> in a mild soap and water solution. Rinse the surface using a second cloth moistened in clean water.

3. DISASSEMBLY

The "Moden" Series Paging Encoder described in this manual can be disassembled to where the circuit boards are exposed or to where the circuit boards are completely removed from the housing. Disassemble the paging encoder as follows:

a. Housing Top Removal

- (1) Disconnect the paging encoder from its power source.
- (2) From the bottom of the housing, remove four screws; refer to Figure 2 for the screw locations.

NOTE

The paging encoder housing (top and bottom) is interconnected by the display circuit board cable.

(3) Carefully remove the top of the housing, and disconnect the keyboard cable from the main circuit board. Refer to Figure 20.

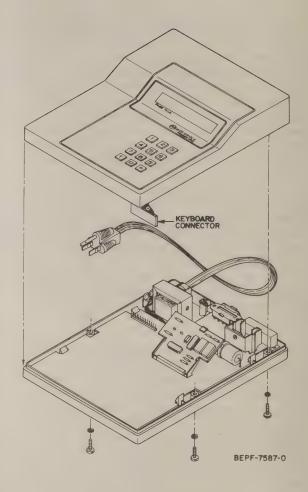


Figure 20. Housing Top Removal

b. Display Circuit Board Removal

- (1) Disengage the spring retaining clip from the top edge of the display circuit board. Refer to Figure 21.
- (2) Grasp the display circuit board holder as shown in Figure 21. Use the thumbs to push on the sides of the circuit board holder to disengage its locking device.
- (3) When the locking device is free from the circuit board and while still applying pressure with the thumbs, use the index fingers to raise the circuit board slightly above the locking device of the circuit board holder.



INSTRUCTION MANUAL REVISION FOR 68P81012C20-0 PAGING ENCODERS REPLACE PAGES 49 & 50 WITH THESE PAGES 49 & 50

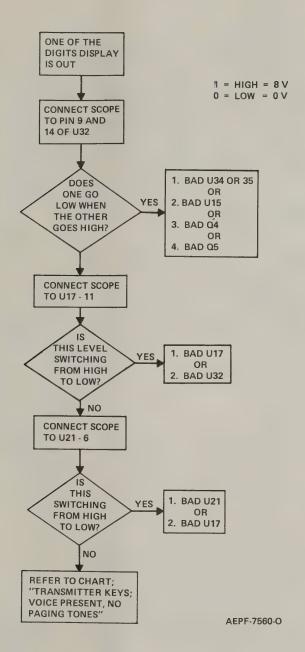


Figure 34. "One of the Digits Display is Out" Troubleshooting Chart

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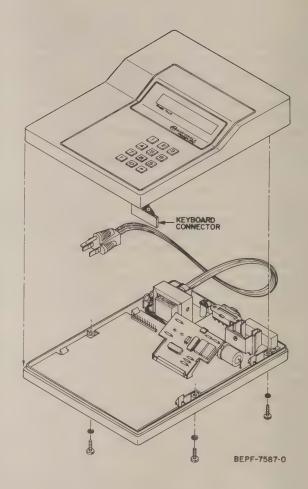


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INSTRUCTION MANUAL REVISION FMR-597D FOR Issue-1 68P81012C20-O PAGING ENCODERS REPLACE PAGES 49 & 50 WITH THESE PAGES 49 & 50

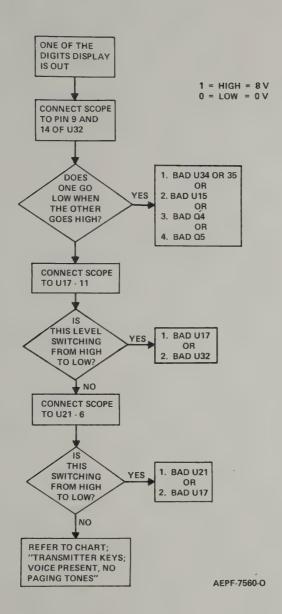
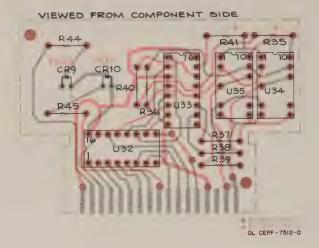


Figure 34.
"One of the Digits Display is Out"
Troubleshooting Chart

DISPLAY CIRCUIT BOARD



DISPLAY CIRCUIT BOARD COMPONENT USAGE

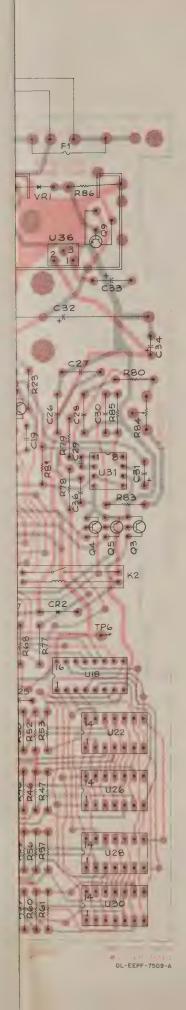
	PAGING ENCODER		
REF. DES.	"MODEN" 100	"MODEN" 36	"MODEN" ALERT CENTRAL
CR10 R45 U35	USED USED USED	NOT USED NOT USED USED	NOT USED NOT USED NOT USED

EPF-7780-0

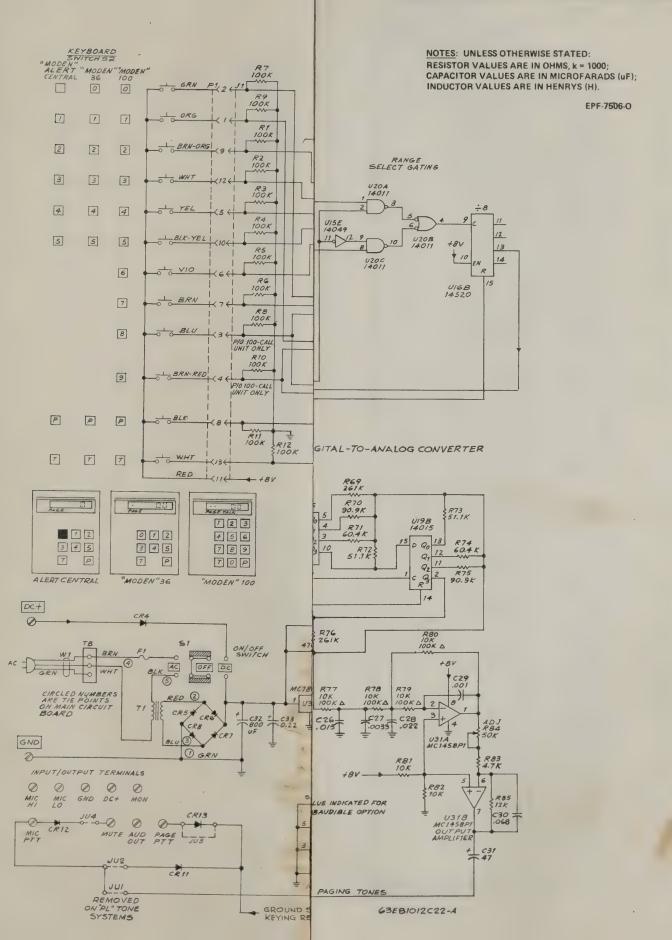
MAIN CIRCUIT BOARD COMPONENT USAGE

REF.	PAGING ENCODER			
DES.	"MODEN"	"MODEN"	ALERT	
	100	36	CENTRAL	
C15	USED	NOT USED	NOT USED	
C16	USED	NOT USED	NOT USED	
Q4	USED	USED	NOT USED	
Q8	USED	NOT USED	NOT USED	
R22	USED	NOT USED	NOT USED	
R31	USED	NOT USED	NOT USED	
R42	USED	USED	NOT USED	
U4	USED	USED	NOT USED	
U6	USED	USED	NOT USED	
U26	USED	NOT USED	NOT USED	
U30	USED	NOT USED	NOT USED	

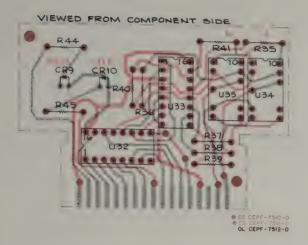
EPF-7781-A



PAGING ENCODERS
REPLACE PAGES 51 & 52 WITH THESE PAGES 51 & 52



DISPLAY CIRCUIT BOARD



DISPLAY CIRCUIT BOARD COMPONENT USAGE

	PAGING ENCODER		
REF.	"MODEN"	"MODEN"	"MODEN" ALERT CENTRAL
DES.	100	36	
CR10	USED	NOT USED	NOT USED
R45	USED	NOT USED	NOT USED
U35	USED	USED	NOT USED

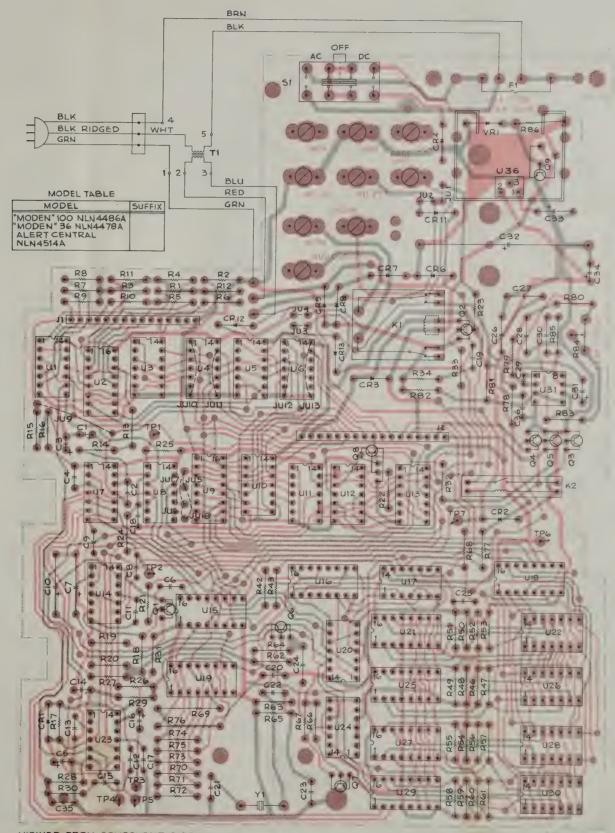
EPF-7780-0

MAIN CIRCUIT BOARD COMPONENT USAGE

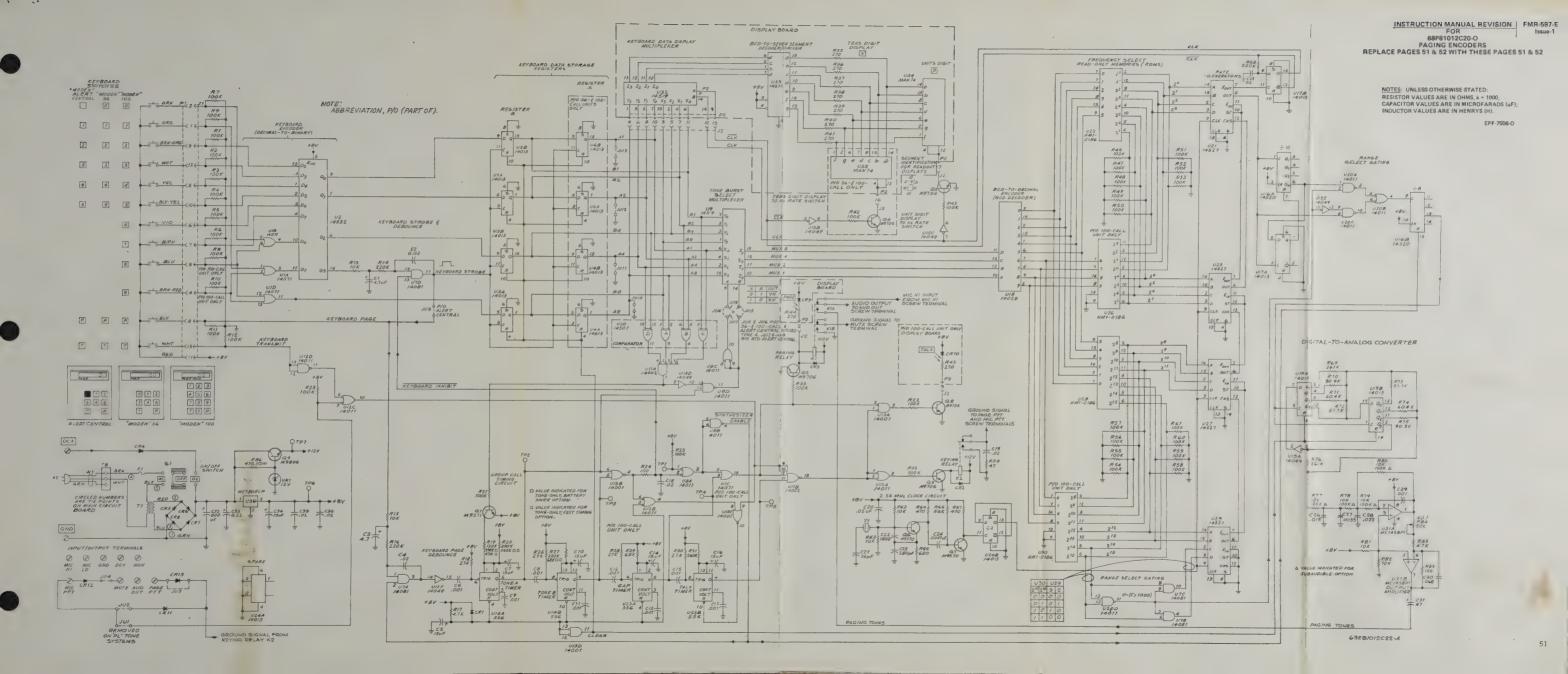
REF.	PAGING ENCODER		
DES.	"MODEN" 100	"MODEN" 36	ALERT CENTRAL
C15	USED	NOT USED	NOT USED
C16	USED	NOT USED	NOT USED
Q4	USED	USED	NOT USED
Q8	USED	NOT USED	NOT USED
R22	USED	NOT USED	NOT USED
R31	USED	NOT USED	NOT USED
R42	USED	USED	NOT USED
U4	USED	USED	NOT USED
U6	USED	USED	NOT USED
U26	USED	NOT USED	NOT USED
U30	USED	NOT USED	NOT USED

EPF-7781-A

MAIN CIRCUIT BOARD



VIEWED FROM COMPONENT SIDE



68PB1012C20-0 PAGING ENCODERS REPLACE PAGES 49 & 50 WITH THESE PAGES 49 & 50

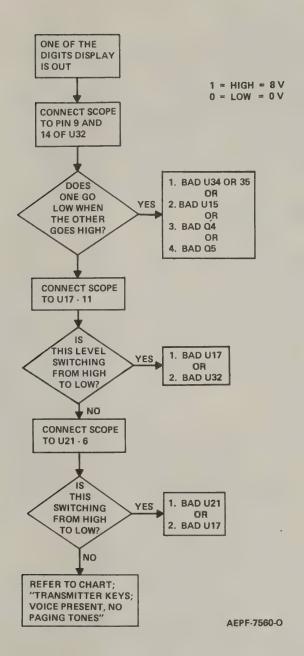


Figure 34.
"One of the Digits Display is Out"
Troubleshooting Chart

Mother Board Kita: NLN448bA Moden 100 NLN4478A Moden 36 NLN4514A Alert Central

PLF-1178-A

SYMBOL PART NO. DESCRIPTION	REFERENCE	MOTOROLA	
C1			DESCRIPTION
10.0 Y unless stated			
C1			CAPACITOR, Fixed: pF ± 5%
C3	61	*********	100 V unless stated
C3			4. / u.F. +20%; 20 V
CS			4 7 uF +20%, 20 V
CS		2182428B18	02 vF-40 460%
Call 12, 13 Call 1			15 uF +20%: 20 V
Call 12, 13 Call 1	C6		1000 +10%; 200 V
Call 12, 13 Call 1		2382783B24	15 uF; 25 V
C11, 12, 13 C13, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12	C8, 9		1000 ±10%; 200 V
100			15 uF; 25 V
100	C11, 12, 13		1000 ±10%; 200 V
C18, 19, 20			15 uF +20%; 20 V
C18, 19, 20			1000 ±10%; 200 V
C21			1000 A10%: 200 V
C21			.02 uF =40 +60%
C22	C21	2184426B16	36: 500 V
C24	CZZ		1500
C25 2182428B18 .02 uF -40 +60% C26 0882905025 .033 uF C28 0882905025 .0033 uF C29 2182218D8 .000 uP C30 0882905020 .200 uP C31 2383441B32 .060 uP C32 238397D06 .068 uF; 50 V C34 2383441B32 .200 mP C34 2383441B21 .20%; 20 V C34 2383441B21 .20%; 20 V C35, 36 2182428B18 .02 uF ±20%; 35 V CR1, 2, 3 4883654H01 .81licon CR1, 12, 13 4882469H13 .01 GR1, 2, 3 4882649H13 .01 M2 8005382E01 .02 uF J1 .0905382E01 .0905382E01 J2 .0905382E01 .0005385E01 J2 .0008385901 .0008385901 M2 .00086971 .00086971 Q2 .00087970 .00087970 R1 .0000124C07 .00087970 R1			280; 500 V
C26			.0047 uF
C27 0882905025 .0033 uF C28 0882905020 .202; 50 V C30 0882905020 .008 uF; 50 V C31 2383441832 .0882950504 .088 uF; 50 V C32 2383441832 .087 ± 20%; 20 V .02 uF ± 20%; 30 V C34 23834418242 .15 ± 20%; 20 V .22 uF ± 20%; 35 V C34 23834418242 .15 ± 20%; 20 V .02 uF C34 23834418242 .15 ± 20%; 20 V .02 uF C34 23834418242 .15 ± 20%; 20 V .02 uF C81, 2, 3 4881654401 .02 uF .02 uF CR1, 12, 13 4882460H13 .51 icon .51 icon Silicon .02 uF .02 uF .02 uF L1 .0905382E01 .05 uF .05 uF L2 .050384E01 .05 uF .05 uF L2 .05385E01 .15 uF .05 uF L2 .05086970 .07 uF .07 uF C9 .05086970 .07 uF .07 uF R1 thru 12 </td <td>C25</td> <td></td> <td>.02 uF -40 +60%</td>	C25		.02 uF -40 +60%
C28			.015 uF; 50 V
C29	C27	088Z905G25	.0033 uF
C30			1000
C31			.068 nF: 50 V
C34			47 uF +20%: 20 V
C34			800 uF -10 +70%; 30 V
C35, 36 C84 thru 8 CR1, 2, 3 CR4 thru 8 CR11, 12, 13 A882466H13 Silicon Silicon Silicon Silicon JACK: Connector Connector Connector Connector Connector Connector Connector Connector Connector TRANSISTOR: See Note I PhP: type M9570 A800869701 A800869700 A80086	C33	2383397D06	
CR1, 2, 3 CR4 thru 8 CR1 thru 8 CR1 1, 12, 13 A882466113 Silicon Sil		2383441B26	15 ± 20%; 20 V
CR1, 2, 3 CR4 thrus 8 CR11, 12, 13 4882466H13 J1 0905382E01 Silicon Silicon Silicon Silicon Silicon Silicon Silicon JACK: Connector RELAY: 2-pole Form C 2-pole Form C 1-pole Form C 4800859701 A800869701 NPN: type M9570 NPN: type M95	C35, 36	2182428B18	.02 uF
CR1, 2, 3 CR4 thrus 8 CR11, 12, 13 4882466H13 J1 0905382E01 Silicon Silicon Silicon Silicon Silicon Silicon Silicon JACK: Connector RELAY: 2-pole Form C 2-pole Form C 1-pole Form C 4800859701 A800869701 NPN: type M9570 NPN: type M95			
CR4 thru 8 CR11,12,13 4882466413 Silicon JACK: Connector RELAY: 2-pole Form C 1-pole Form C 1-pole Form A 4800859571 Q2 thru 5 4800869570 Q8 4800869570 Q9 480086970 R1 thru 12 R1 thru 12 R1 d600124C97 R1 d600124A73 R14 0600124A73 R15 0600124A73 R16 0600124A73 R17 R18 0600124B06 R17 R18 0600124B06 R18 0600124C97 R19 R19 0600124C97 R19 R20 0600124C93 R21 C20 C50 C50 C50 C50 C50 C50 C50 C50 C50 C5	an		DIODE: See Note I
CR11,12,13	CR1, 2, 3		
Jack: Connector RELAY: 2-pole Form C 1-pole Form C	CR4 thru 8		
No.	CR11, 12, 13	4002400113	Sincon
No.			JACK:
No.	J1	0905382E01	Connector
No.			
TRANSISTOR: See Note I PNP: type M9571 NPN: type M9570 NPN			RELAY:
TRANSISTOR: See Note I PNP: type M9571 NPN: type M9570 NPN			2-pole Form C
01 4800869571 PNP: type M9571 02 thru 5 4800869570 NPN: type M9570 08 4800869570 NPN: type M9570 09 4800869570 NPN: type M9570 NPN: type M	K2	8005385E01	1-pole Form A
01 4800869571 PNP: type M9571 02 thru 5 4800869570 NPN: type M9570 08 4800869570 NPN: type M9570 09 4800869570 NPN: type M9570 NPN: type M			mnavarana a v
22 thru 5 6800869706 RSPN: type M95707 Q8 4800869706 A800869706 RSPN: type M9570 RSPN: type M9570 RSPN: type M9806 RSSISTOR, Fixed: x ±10% 1/4 W unless stated 10.5% RSSISTOR, Fixed: x ±10% 1/4 W unless stated 10.5% RSSISTOR, Fixed: x ±10% 1/4 W unless stated 10.5% RSSISTOR, Fixed: x ±10% 1/4 W unless stated 10.5% RSSISTOR, Fixed: x ±10% 1/4 W unless stated 12.5%	0)	4000060572	DND: Mars Mos 71
New			NPN: type M9706
Q9 4800869806 NPN; type My806 RESISTOR, Fixed: \(\(\) + \(\) 1/4 W unless stated \) 1/4 W unless stated \) 1/6 W \(\) 5% 1/7 W \(Q6. 7		NPN: type M9570
Q9 4800869806 NPN; type My806 RESISTOR, Fixed: \(\(\) + \(\) 1/4 W unless stated \) 1/4 W unless stated \) 1/6 W \(\) 5% 1/7 W \(Q8		NPN; type M9706
R] thru 12 0600124C97 100k R13 0600124A73 10k ±5% R15 0600124A73 10k ±5% R15 0600124A73 10k ±5% R16 0600124A73 10k ±5% R17 0600124C65 4, 7k R18 0600124C65 4, 7k R19 0600124C65 12 20k ±5% R21 0200124C65 100 R22 0600124A99 120k ±5% R24 0600124A99 100k ±5% R25 0600124C97 100k R25 0600124C97 100k R26 0600124C97 100k R27 0600124C83 27k R28 0600124C97 100k R29 0600124C97 100k R29 0600124C83 100 R20 0600124C83 100 R21 0600124C83 100 R22 0600124C83 100 R23 0600124C83 100 R24 0600124C83 100 R25 0600124C83 100 R26 0600124C83 100 R27 0600124C83 100 R27 0600124C83 100 R28 0600124C83 100 R29 0600124C83 100 R29 0600124C83 100 R29 0600124C83 100 R29 0600124C97 100k R29			NPN; type M9806
R1 thru 12 0600124C97 100K R13 0600124A73 10k ±5% R14 0600124B00 220k ±5% R15 0600124A73 10k ±5% R16 0600124A73 10k ±5% R17 0600124C65 4, 7k R18 0600124C65 4, 7k R19 0600124C65 4, 7k R20 0600124C83 120k ±5% R21, 22, 23 0600124C97 100K R24 0600124C97 100K R24 0600124C97 100K R25 0600124C97 100K R26 0600124C97 100K R27 0600124C97 100K R28 0600124C97 100K R29 0600124C97 100K R29 0600124C97 100K R29 0600124C97 100K R29 0600124C97 100K R31 0600124C97 100K R32 0600124C97 100K R33 0600124C97 100K R34 0600124C97 100K R34 0600124C97 100K			
R1 thru 12 0600124C97 100K R13 0600124A73 10k ±5% R14 0600124B00 220k ±5% R15 0600124A73 10k ±5% R16 0600124A73 10k ±5% R17 0600124C65 4, 7k R18 0600124C65 4, 7k R19 0600124C65 4, 7k R20 0600124C83 120k ±5% R21, 22, 23 0600124C97 100K R24 0600124C97 100K R24 0600124C97 100K R25 0600124C97 100K R26 0600124C97 100K R27 0600124C97 100K R28 0600124C97 100K R29 0600124C97 100K R29 0600124C97 100K R29 0600124C97 100K R29 0600124C97 100K R31 0600124C97 100K R32 0600124C97 100K R33 0600124C97 100K R34 0600124C97 100K R34 0600124C97 100K			RESISTOR, Fixed: A ±10%
R13 0600124A73 10k ±5% R15 0600124A73 10k ±5% R15 0600124A73 10k ±5% R17 0600124C65 4 + 7k R18 18 0600124C63 27k R219 0600124A99 120k ±5% R210 0600124A99 120k ±5% R210 0600124A99 100k R25 0600124C97 100k R25 0600124C97 100k R26 0600124C97 100k R27 0600124C97 100k R28 0600124C97 100k R28 0600124C97 100k R29 0600124C93 6 + 5% R29 0600124C93 6 + 5% R29 0600124C93 5 + 5% R29 0600124C93 6 + 5% R29 0600124C93 7 + 00k R29 0600124C97 100k R2			1/4 W unless stated
R15			
R15			10k ±5%
R16 0600124B06 220k ±5% R17 0600124C65 4, 7% R18 0600124C63 27k R19 0600124C497 100k R21, 22, 23 0600124C97 100k R24 0600124C97 100k R25 0600124C47 100k R26 0600124C47 100k R27 0600124C47 100k R28 0600124C47 100k R28 0600124C47 100k R29 0600124C97 100k R29 0600124C97 100k R29 0600124C97 100k R31 0600124C9 100k R31 0600124C9 100k R32 0600124C9 100k R33 0600124C9 100k R34 0600124C9 10			10k +5%
R17 0600124C65 4, 7k R18 0600124C63 27k R19 0600124A99 120k ±5% R20 0600124B12 300k ±5% R21, 22, 23 0800124C97 100k R25 0600124C25 100 R25 0600124C48 27k R27 0600124C48 27k R27 0600124C8 27k R28 0600124C8 27k R29 0600124C8 27k R29 0600124C8 27k R31 0600124C8 27k R31 0600124C8 27k R31 0600124C8 27k R32 0600124C8 27k R33 0600124C8 27k R34 0600124C8 27k R35 0600124C8 27k R36 28 28 28 28 28 28 28 28 28 28 28 28 28			220k +5%
R18			4.7k
R21, 22, 23 0600124C97 100k R24 0600124C97 1000 R25 0600124C4C97 1000 R26 0600124C483 27k R27 0600124C83 27k R28 0600124C83 27k R29 0600124C83 27k R31 0600124C83 27k R31 0600124C83 27k R31 0600124C48 27k R32, 33 0600124C48 27k R34 0600124C47 1000	R18	0600124C83	27k
R21, 22, 23 0600124C97 100k R24 0600124C97 1000 R25 0600124C4C97 1000 R26 0600124C483 27k R27 0600124C83 27k R28 0600124C83 27k R29 0600124C83 27k R31 0600124C83 27k R31 0600124C83 27k R31 0600124C48 27k R32, 33 0600124C48 27k R34 0600124C47 1000	R19		120k ±5%
R21, 22, 23 0600124C97 100k R24 0600124C97 1000 R25 0600124C4C97 1000 R26 0600124C483 27k R27 0600124C83 27k R28 0600124C83 27k R29 0600124C83 27k R31 0600124C83 27k R31 0600124C83 27k R31 0600124C48 27k R32, 33 0600124C48 27k R34 0600124C47 1000	R20		390k ±5%
R25 0x00124C97 100k R26 0x00124B06 27k R27 0x00124B06 220k ±5% R28 0x00124C83 27k R39 0x00124A93 68k ±5% R31 0x00124C83 27k R31 0x00124B16 560k ±5% R32 33 0x00124C97 100k R34 0x00124C17 47 R42 43 0x00124C17 40k	R21, 22, 23		
R26			
R27 06.00124B06 2200k.55% R28 0600124C83 27k R39 0600124C83 27k R31 0600124C83 27k R31 0600124B16 560k.±5% R32, 33 0600124C97 1000k R34 0600124C17 47		0600124097	
R28 0600124C83 27k R29 0600124A93 68k ±5% R30 0800124C83 27k R31 0600124B10 560k ±5% R32, 33 0600124C97 100k R34 0600124C17 47 R42, 43 0600124C97 100k			
R29 0600124A93 68k ±5% R30 0600124C83 27k R31 0600124B16 560k ±5% R32, 33 0600124C97 1000 R34 0600124C17 47 R42, 43 0600124C17 47			27k
R30 0600124G83 27k R31 0600124B16 560k±5% R32, 33 0600124C97 100k R34 0600124G17 47 R42, 43 0600124G97 100k			
R31 0600124B16 560k ±5% R32, 33 0600124G97 100k R34 0600124G17 47 R42, 43 0600124G97 100k			27k
R32, 33 0600124C97 100k R34 0600124C17 47 R42, 43 0600124C97 100k	R31	0600124B16	560k <u>+</u> 5%
R34 0600124C17 47 R42, 43 0600124C97 100k	R32, 33		100k
R4Z, 43 0600124C97 100k	R34		
	R42, 43		100k 100k
R62, 63 0600124A73 10k ±5% 470 470			470
R65 0600124C45 680		0600124C45	
R66 0600124C91 56k			
R67 0600124C41 470			
R68 0600124B06 220k			
R69 0682672B99 261k ±1%	R69	0682672B99	261k ±1%

R70 R71	0683175C76 0683175C64	90. 9k ±1%
R72, 73	0683175C64	60.4k ±1%
R74	0683175C64	51. 1k ±1% 60. 4k ±1%
R75	0683175C76	60.4k ±1% 90.9k ±1%
R76	0682672B99	261k ±1%
R77 thru 82	0600124A73	10k +5%
R83	0600124C65	4.7k
R84	1883083G26	pot, 50k
R85 R86	0600124C75	12k
Kae	0600125A41	470 ±5%; 1/2 W
Sı	4005381E01	SWITCH: Slide
Uı	5182822F43	INTEGRATED CIRCUIT: Quad Z-Input AND Gate, type MC14071CP
U2	5182822F51	8-Bit Priority Encoder,
U3 thru 6	5182822F10	type MC14532CP Dual D-Type Flip-Flop,
דטז	5182822F44	type MC14013CP Quad 2-Input OR Gate,
U8	5182822F08	type MC14081CP
		Quad 2-Input NAND Gate, type MC14011CP
U9	5182822F28	4-Bit and/or Select, type MC14519CP
U10	5182822F18	Quad Exclusive OR Gate, type MC14507CP
Ull	5182822F25	Dual 4-Input NOR Gate, type MC14002CP
Ul2	5182822F08	Quad 2-Input NAND Gate, type MC14011CP
U13	5182822F03	Quad 2-Input NOR Gate, type MC14001CP
U14	5184320A85	Dual Timer,
U15	5182822F40	type NE556A Hex Buffer (Inverting),
U16	5182822F34	type MC14049CP Dual Binary Up Counter,
U17	5182822F10	type MC14520CP Dual D-type Flip-Flop,
U18	5182822F47	type MC14013CP MC14028CP
U19	5182822F11	Dual 4-Bit Static Shift Register, type MC14015CP
U20	5182822F08	Quad 2-Input NAND Gate, type MC14011CP
U21	5182822F52	BCD Rate Multiplier, type MC14527CP
U22, 26, 28, 30		Factory Programmed Read-Only Memory (See Note II)
U23 U24	5184320A85 5182822F10	Dual Timer, type NE556A Dual D-Type Flip-Flop,
U25	5182822F52	type MC14013CP BCD Rate Multiplier,
U27	5182822F52	type MC14527CP BCD Rate Multiplier,
U27		type MC14527CP
/	5182822F52	BCD Rate Multiplier, type MC14527CP
U31 U36	5184320A12 5184621K16	type N5558V Voltage Regulator, type MC7808
VRI	4882256C25	DIODE: See Note I Zener, 12 V
Y1	4805386E01	CRYSTAL: See Note III Resonator
	NONREFERENCI	ED ITEMS
	0105957C50	BOARD and TERMINAL
	0705387E01	SUPPORT
	0905261D05	CONNECTOR, Wafer
	0905382E01	CONNECTOR
	0905388E02	SOCKET, IC
	1405383E01	INSULATOR, Fuse
	2605380E01	HEAT SINK
	1405474E01	SHIELD, Switch
	4210122A12	CLIP, Retaining STRAP, Cable Harness STRAP, Cable Harness
	4210217A02	STRAP, Cable Harness
	4210217A02	STRAP, Cable Harness

Top Cover Kits: NLN4487A Moden 100 NLN4480A Moden 36

NLN4480A M NLN4483A A		PLF-1179-0
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
P1	0905259D01	PLUG: Board Connector
S2	4005378E01	SWITCH: 12-Position Keyboard
	NONREFERENC:	ED ITEMS
	0200877296 0210101 A45 0210101 A45 0210101 A45 0300007362 0400007550 1305349E01 or 1305349E02 or 1305349E03 22905260D01 3805352E01 3805352E03 3805352E11 3805352E10	NUT, Elastic Stop: 2-56 NUT, Spring Type U NUT, Steel; Plain SCREW, 6-3-5 x 1/2 LOCKWASHER #6 ESCUTCHEDON, Keyboard (NLEN487A) ESCUTCHEON, Keyboard (NLEN489A) ESCUTCHEON, Keyboard (NLEN490A) ESCUTCHEON, Keyboard (NLEN490A) ESCUTCHEON, Keyboard (NLEN490A) ESCUTCHEON, Keyboard ESCUTCHEON, ESCUTCHEON ESCUTCHEON, ESCUTCHEON ESCUTCHEON, ESCUTCHEON ESCUTCHEON, ESCUTCHEON

Display Readout Kits: NLN4488A Moden 100 NLN4481A Moden 36

NLN4515A	Alert Central	PLF-1180-0
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
CR9, 10	4805389E01	DIODE: See Note I LED, Indicator
R35 thru 41 R44, 45	0600124C35	RESISTOR, Fixed: A 270 ±10%; 1/4 W
U32	5182822F28	INTEGRATED CIRCUIT: 4-Bit AND/OR Select Gate; type MC14519CP
U33 U34, 35	5182822F06 4883477K01	BCD to 7-Segment Latch/ Decoder/Driver; type MC14511CP 7-Segment Diode Array
	NONREFERENC	ED ITEM
	8405307E01	CIRCUIT BOARD, LED Display

NOTES:

- For optimum performance, order replacement diodes and transistors by Motorola part number
- II. When ordering ROM's, specify ROM Kit number: NLN1442A for "Moden" 100 and NLN1435A for "Moden" 36 and Alert Central. Also, specify tone group to be programmed.
- III. When ordering crystal units, specify operating frequency, crystal frequency, and part number (type).

NLN4484A S	ubaudible Option	PLF-1176-0
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R77 thru 80	0600124A97	RESISTOR, Fixed: A 100k ±5%; 1/4 W

NLN4485A Tone-Only Battery Saver Option		ver Option PLF-1177-0
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R19 R20 R27	0600124B12 0600124B16 0600124A93	RESISTOR, Fixed: A 390k ±5%; 1/4 W 560k ±5%; 1/4 W 68k ±5%; 1/4 W

Base and Transformer Kits: NLN4479A 115 V (Standard)

	0 V (Optional)	PLF-1181-C
REFERENCE SYMBOL	MOTOROLA PART NO,	DESCRIPTION
Fl	6500139681 or 6500139680	FUSE: 1/8-Amp., 125 V (NLN4479A) 1/16-Amp., 250 V (NLN4535A)
Tl	2505379E01 or 2505379E02	TRANSFORMER: Power (NLN4479A) Power (NLN4535A)
W1	3005284A02	AC CORD & PLUG: 3-Conductor
	NONREFERENC	ED ITEMS
	0200001362 0300007229 0400001719 0400007666 1505348E01 3100120365 4210217A02 4210283A20 4282387D05	NUT, 6-32 x 1/4" x 3/32" SCREW, 6-32 x 3/8 WASHER, Flat LOCKWASHER #6 COVER, Bottom STRIP, Terminal STRAP, Cable Harness CLIP, Cable (Nylon) CLAMP, Cable

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R19	0600124A89	RESISTOR, Fixed: <u>n ±10%</u> 47k +5%; 1/4 W
R20	0600124B16	560k +5%; 1/4 W
R27	0600124A93	68k +5%; 1/4 W

52 PARTS LISTS

INSTRUCTION MANUAL REVISION FMR-597D FOR Issue-2 68P81012C20-O PAGING ENCODERS REPLACE PAGES 49 & 50 WITH THESE PAGES 49 & 50

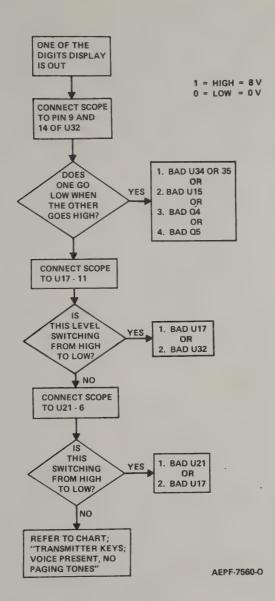
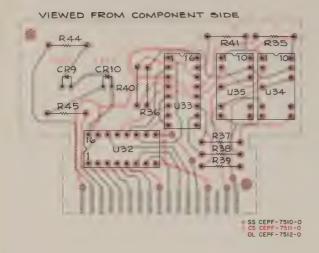


Figure 34.
"One of the Digits Display is Out"
Troubleshooting Chart

DISPLAY CIRCUIT BOARD



DISPLAY CIRCUIT BOARD COMPONENT USAGE

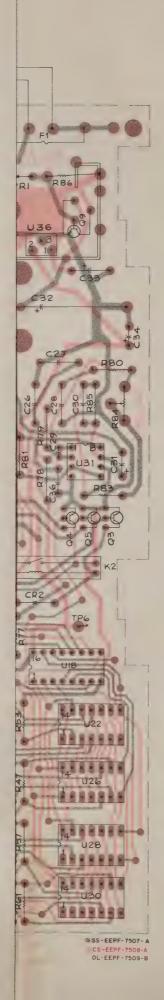
	PAGING ENCODER		
REF.	"MODEN"	"MODEN"	"MODEN" ALERT CENTRAL
DES.	100	38	
CR10	USED	NOT USED	NOT USED
R45	USED	NOT USED	NOT USED
U35	USED	USED	NOT USED

EPF-7780-0

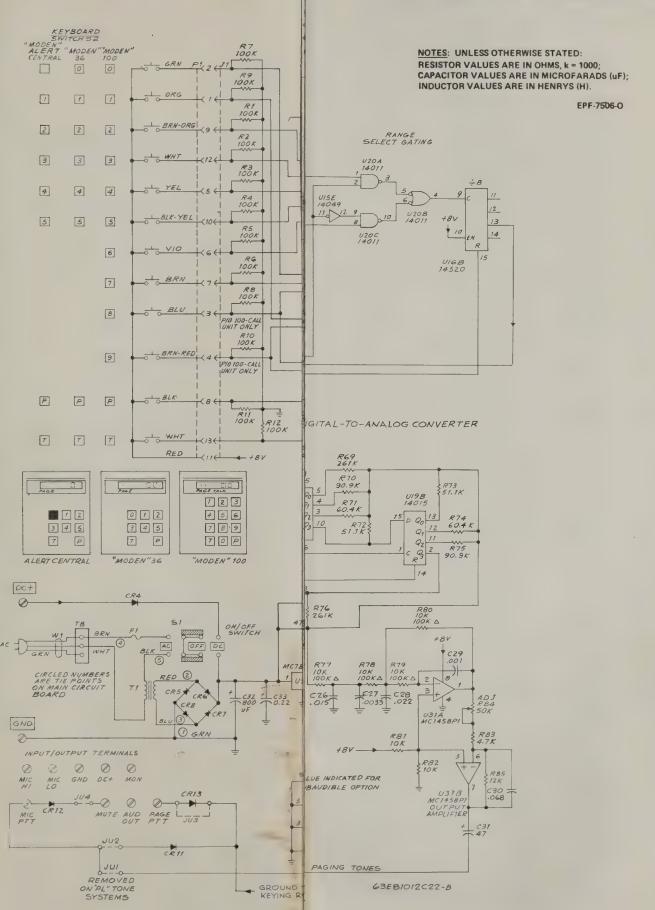
MAIN CIRCUIT BOARD COMPONENT USAGE

REF. DES.	PAGING ENCODER			
	"MODEN" 100	"MODEN" 36	ALERT CENTRAL	
C15	USED	NOT USED	NOT USED	
C16	USED	NOT USED	NOT USED	
Q4	USED	USED	NOT USED	
Q8	USED	NOT USED	NOT USED	
R22	USED	NOT USED	NOT USED	
R31	USED	NOT USED	NOT USED	
R42	USED	USED	NOT USED	
U4	USED	USED	NOT USED	
U6	USED	USED	NOT USED	
U26	USED	NOT USED	NOT USED	
U30	USED	NOT USED	NOT USED	

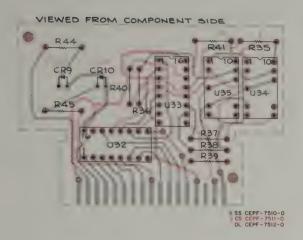
EPF-7781-A



68PB1012C20-O PAGING ENCODERS REPLACE PAGES 51 & 52 WITH THESE PAGES 51 & 52



DISPLAY CIRCUIT BOARD



DISPLAY CIRCUIT BOARD COMPONENT USAGE

REF. DES.	PAGING ENCODER		
	"MODEN" 100	"MODEN" 36	"MODEN" ALERT CENTRAL
CR10 R45 U35	USED USED USED	NOT USED NOT USED USED	NOT USED NOT USED NOT USED

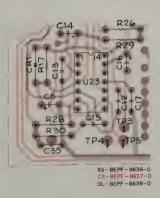
EPF-7780-0

MAIN CIRCUIT BOARD COMPONENT USAGE

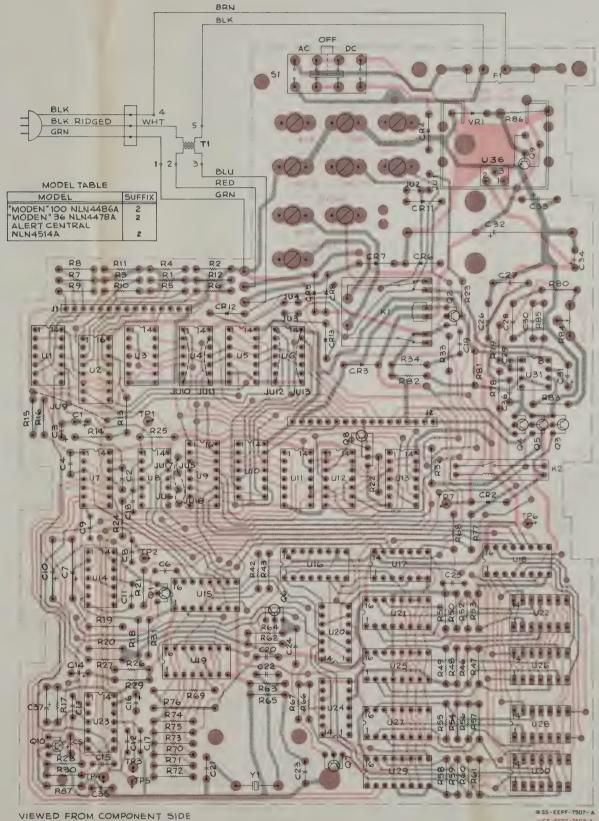
REF. DES.	PAGING ENCODER			
	"MODEN"	"MODEN" 36	ALERT	
C15	USED	NOT USED	NOT USED	
C16	USED	NOT USED	NOT USED	
Q4	USED	USED	NOT USED	
0.8	USED	NOT USED	NOT USED	
R22	USED	NOT USED	NOT USED	
R31	USED	NOT USED	NOT USED	
R42	USED	USED	NOT USED	
U4	USED	USED	NOT USED	
U6	USED	USED	NOT USED	
U26	USED	NOT USED	NOT USED	
U30	USED	NOT USED	NOT USED	

EPF-7781-A

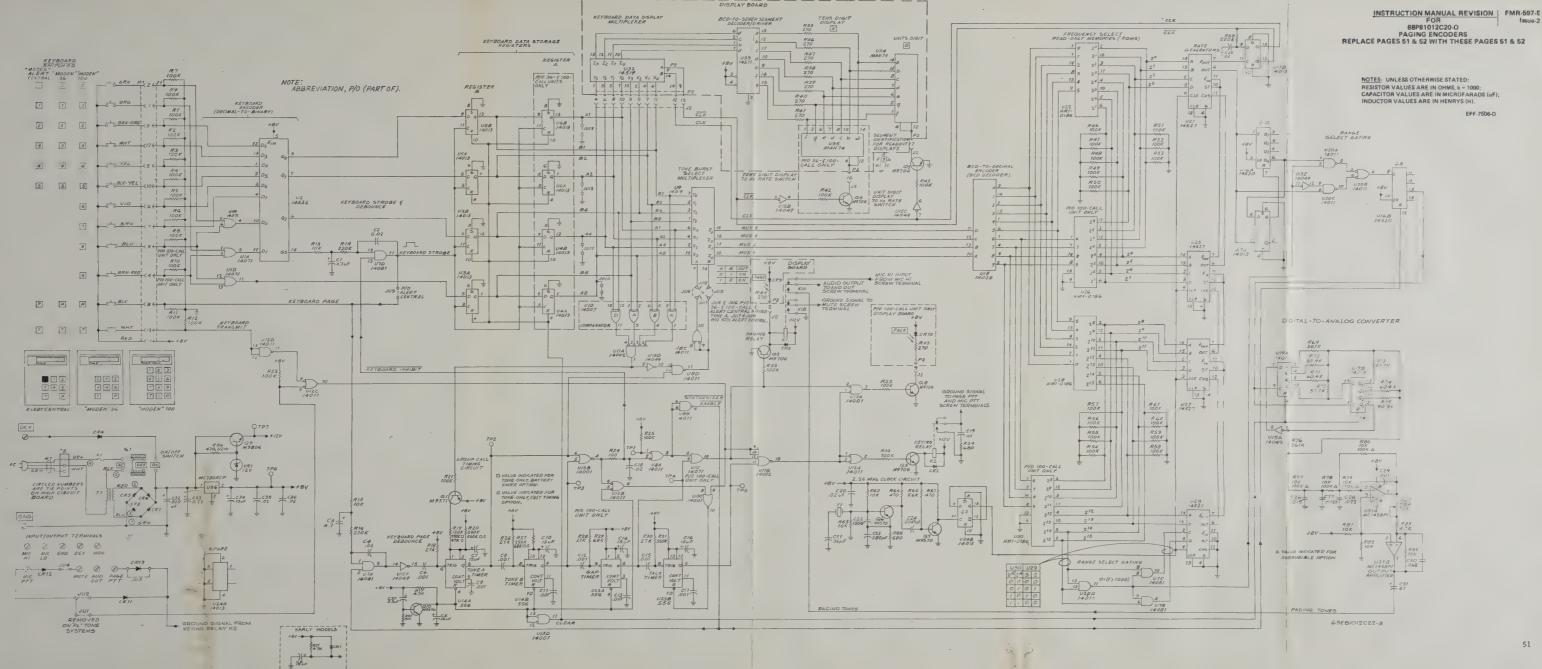
FOR MODELS
NLN4486A-1 & earlier
NLN4478A-1 & earlier
NLN4514A-1 & earlier



MAIN CIRCUIT BOARD



- CS-EEPF-7508-A OL-EEPF-7509-B





MANUAL USER QUESTIONNAIRE

We believe that reports from users provide valuable information for producing good service manuals. Your answers and comments on the following questionnaire will aid us in writing manuals that contain information of maximum benefit to you.

	In reference to Manual No. 68P	
First Fold	DIAGRAMS (indicate diagram number/description)	First _
	Are adequate	7 010
	Are too small too big	
	Should contain the following additional information:	
	Contain the following errors:	
	PARTS LISTS	
	Are adequate	
	The following information is incorrect or should be added:	
	I prefer exploded views for parts identification	
Second	THEORY/TROUBLESHOOTING INFORMATION	Second
Fold	I use troubleshooting charts frequently.	Fold
	I do not use troubleshooting charts.	
	I prefer tabular symptom/remedy charts.	
	The following information should be added (or corrected):	
	MODEL CHARTS	
	I use charts to determine if manual is applicable to my radio model.	
	I use the charts to determine content of model or identify what chassis/kits are in the model; or:	
	I do not use these charts.	

Mother Board Kits: NLN4486A Moden 100 NLN4478A Moden 36 NLN4514A Alert Central

PLF-1178-B

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		CAPACITOR, Fixed: pF ± 5%
		100 V unless stated
Cl	2383441B18	4.7 uF +20%; 20 V .02 uF +40 +60% .02 uF +40 +60% .02 uB +40 +60% 15 uF +20%; 20 V 1000 -10%; 20 V .01 uF -40 +60% 36; 500 V 1000 -10%; 20 V .02 uF -40 +60% .03 uF -40 +60% .03 uF -40 +60% .03 uF -40 +60% .03 uF -40 +60%
C2 C3	2181428B18 2383441B18	.02 uF-40 +60%
C4	2182428B18	02 HF-40 +60%
C5	2383441B26	15 uF +20%; 20 V
C6	2182187B20	1000 ±10%; 200 V
C7	2382783B24	15 uF; 25 V
C8, 9 C10	2182187B20 2382783B24	1000 ±10%; 200 V
C11, 12, 13	2182187B20	1000 +10%: 200 V
C14	2383441B26	15 uF +20%; 20 V
C15	2182187B20	1000 +10%; 200 V
Clb	2383441B26	15 uF +20%; 20 V
C17	2182187B20	1000 ±10%; 200 V
C18	2182428B18 2182428B62	01 uF -20+80%: 200 V
C20	2182428B18	.02 uF -40+60%
C21	2184426B16	36; 500 V
C22	2184426B63	1500
C23	2184426B54	280; 500 V
C24 C25	0882905G26 2182428B18	.0047 uF
C26	0882905G10	.02 uF -40 +60% .015 uF; 50 V
C27	0882905G25	.0033 uF
C28	0882905G02	.022; 50 V
C29	2182213E08	
C30 C31	0882905G04 2383441B32	.068 uF; 50 V
C32	2383441B32 2382077C29	800 vF -10 +20%; 20 V
C33	2383397D06	.068 uF; 50 V 47 uF ±20%; 20 V 800 uF -10 +70%; 30 V 0.22 uF ±20%; 35 V 15 ± 20%; 20 V
C34	2383441B26	15 + 20%; 20 V
C35, 36	1 2182428B18	.02 uF 3.3 uF ±20%; 25 V
C37	2383397D01	3.3 uF ±20%; 25 V
CP2 3	4883654H01	DIODE: See Note I
CR2, 3 CR4 thru 8	4882466H13	Silicon
CR11, 12, 13	488Z466H13	Silicon
11	0905382E01	JACK: Connector
JI	0905382E01	Connector
		RELAY:
K1	8005384E01	2-pole Form C 1-pole Form A
K2	8005385E01	1-pole Form A
		TRANSISTOR: See Note I
QI	4800869571	TRANSISTOR: See Note I
Q2 thru 5	4800869706	PNP; type M9571 NPN; type M9706 NPN; type M9570
Q6, 7	4800869570	NPN; type M9570
Q8	4800869706	NPN: type M9706
Q9 Q10	4800869806 4800869570	NPN; type M9706 NPN; type M9806 NPN; type M9570
410	4800007370	RESISTOR, Fixed: A ±10%
		1/4 W unless stated
R1 thru 12	0600124C97	100k
R13	0600124A73	10k ±5%
R14 R15	0600124B06 0600124A73	220k +5% 10k +5%
R16	0600124B06	10k ±5% 220k ±5%
R17	0600124C65	20k ±5% 4.7k 27k 120k ±5% 390k ±5%
R18	0600124C83	27k
R19	0600124A99	120k +5% 390k +5%
R20 R21, 22, 23	0600124B12 0600124C97	390k ±5% 100k
R24	0600124C25	100
R25	0600124C97	100k
R26	0600124C83	27k
R27	0600124B06	220k ±5%
R28 R29	0600124C83 0600124A93	27k 68k <u>+</u> 5%
R30	0600124C83	27k
R31	0600124B16	560k ±5%
R32, 33	0600124C97	100k
R34	0600124C45	680
R42, 43 R46 thru 61	0600124C97 0600124C97	100k 100k
R62, 63	0600124C97	10k ±5%
R64	0600124C41	470
R65	0600124C45	680
R66	0600124C91 0600124C41	56k 470
R68	0600124C41	220k
R69	0682672B99	261k ±1%

	4210217A02 4210217A02	HEAT SINK SHIELD, Switch CLIP, Retaining STRAP, Cable Harness STRAP, Cable Harness
	4210122A12	CLIP, Retaining
	2605380E01 1405474E01	SHIELD, Switch
	1405383E01	INSULATOR, Fuse
	0905382E01 0905388E02	CONNECTOR, Wafer CONNECTOR SOCKET, IC INSULATOR, Fuse
	0905261D05 0905382E01	CONNECTOR, Wafer
	0105957C50 0705387E01	BOARD and TERMINAL SUPPORT
	NONREFEREN	
ΥI	4805386E01	CRYSTAL: See Note III Resonator
VRI	4882256C25	DIODE: See Note I Zener, 12 V
U31 U36	5184320A12 5184621K16	type N5558V Voltage Regulator, type MC780
U29	5182822F52	BCD Rate Multiplier, type MC14527CP
U27	5182822F52	type MC14527CP BCD Rate Multiplier, type MC14527CP
U25	5182822F52	type MC14013CP BCD Rate Multiplier,
U23 U24	5184320A85 5182822F10	Dual Timer, type NE556A Dual D-Type Flip-Flop,
U22, 26, 28, 30		type MC14527CP Factory Programmed Read-On Memory (See Note II)
U21 ·	5182822F52	type MC14011CP BCD Rate Multiplier,
U20	5182822F08	type MC14015CP . Quad 2-Input NAND Gate,
U18 U19	5182822F47 5182822F11	MC14028CP
U17	5182822F10	Dual D-type Flip-Flop, type MC14013CP
U16	5182822F34	Dual Binary Up Counter, type MC14520CP
U15	5182822F40	type NE556A Hex Buffer (Inverting), type MC14049CP
U14	5184320A85	type MC14001CP Dual Timer,
U13	5182822F03	type MC14011CP Quad 2-Input NOR Gate,
U12	5182822F08	type MC14002CP Quad 2-Input NAND Gate,
Ull	5182822F25	type MC14507CP Dual 4-Input NOR Gate.
U10	5182822F18	type MC14519CP Quad Exclusive OR Gate.
U9	5182822F28	type MC14011CP 4-Bit and/or Select,
U8	5182822F08	type MC14081CP Quad 2-Input NAND Gate.
U7	5182822F44	type MC14013CP Quad 2-Input OR Gate,
U3 thru 6	5182822F10	type MC14532CP
UI UI	5182822F43 5182822F51	Quad 2-Input AND Gate, type MC14071CP 8-Bit Priority Encoder,
Ul	5182822F43	INTEGRATED CIRCUIT: Quad 2-Input AND Gate,
S1	4005381E01	SWITCH: Slide
R86 R87	0600125A41 0600124A73	470 ±5%; 1/2 W 10 k ±5%
R85	0600124C75	12k
R83 R84	0600124C65 1883083G26	4.7k pot, 50k
R77 thru 82	0600124A73	10k +5%
R75 R76	0683175C76 0682672B99	60.4k +1% 90.9k +1% 261k +1%
R72, 73 R74	0683175C60 0683175C64	51.1k +1%
D 72 22		60.4k ±1%
R71	0683175C64	90.9k ±1%

Top Cover Kits: NLN4487A Moden 100 NLN4480A Moden 36

	NLN4483A A	lert Central	PLF-1179-0
	REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	Pl	0905259D01	PLUG: Board Connector
	52	4005378E01	SWITCH: 12-Position Keyboard
i		NONREFERENCE	ED ITEMS
		0200877296	NUT, Elastic Stop; 2-56
-		0210101A25	NUT, Spring Type U
		0210101A44	NUT, Steel; Plain
1		0300007362	SCREW, 6-36 x 1/2
		0400007650	LOCKWASHER #6
		1305349E01	ESCUTCHEON, Keyboard
			(NLN4487A)
		or 1305349E02	ESCUTCHEON, Keyboard
			(NLN4480A)
	ļ.	or 1305349E03	ESCUTCHEON, Keyboard
			(NLN4483A)
		2905260D01	TERMINAL
		3805352E01	KEY TOP, #1
		3805352E02	KEY TOP, #2
		3805352E03	KEY TOP, #3
		3805352E04	KEY TOP, #4
		3805352E05	KEY TOP, #5
		3805352E06	KEY TOP, #6
		3805352E07	KEY TOP, #7
		3805352E08	KEY TOP, #8
		3805352E09	KEY TOP, #9
		3805352E10	KEY TOP, #0
		3805352E11	KEY TOP, Letter T
	,	3805352E12	KEY TOP, Letter P
		3805352E13	KEY TOP, Blank
		4210217A02	STRAP, Cable Harness
		4282143C01	CLAMP, Cable
		5505475E01	KEY, Polarizing
		6105350E01	WINDOW

Display Readout Kits: NLN4488A Moden 100 NLN4481A Moden 36 NLN4515A Alert Central

PLF-1180-0

		1 21 -1100-0
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
CR9, 10	4805389E01	DIODE: See Note I LED, Indicator
R35 thru 41 R44, 45	0600124C35	RESISTOR, Fixed: A 270 ±10%; 1/4 W
U32	5182822F28 5182822F06	INTEGRATED CIRCUIT: 4-Bit AND/OR Select Gate; type MC14519CP BCD to 7-Segment Latch/ Decoder/Driver:
U34, 35	4883477K01	type MC14511CP 7-Segment Diode Array
	NONREFERENCE	ED ITEM
	8405307E01	CIRCUIT BOARD, LED Display

NOTES:

- For optimum performance, order replacement diodes and transistors by Motorola part number
- II. When ordering ROM's, specify ROM Kit number: NLN1442A for "Moden" 100 and NLN1435A for "Moden" 36 and Alert Central. Also, specify tone group to be programmed.
- III. When ordering crystal units, specify operating frequency, crystal frequency, and part number (type).

NLN4484A Subaudible Option PLF-1176-0 REFERENCE MOTOROLA DESCRIPTION SYMBOL PART NO. RESISTOR, Fixed: A R77 thru 80 0600124A97

NLN4485A Tor	NLN4485A Tone-Only Battery Saver Option		
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION	
R19 R20 R27	0600124B12 0600124B16 0600124A93	RESISTOR, Fixed: A 390k ±5%; 1/4 W 560k ±5%; 1/4 W 68k ±5%; 1/4 W	

Base and Transformer Kits: NLN4479A 115 V (Standard)

NLN4535A 230 V (Optional)		PLF-1181-
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
Fl	6500139681 or 6500139680	FUSE: 1/8-Amp., 125 V (NLN4479A) 1/16-Amp., 250 V (NLN4535A)
Tl	2505379E01 or 2505379E02	TRANSFORMER: Power (NLN4479A) Power (NLN4535A)
W1	3005284A02	AC CORD & PLUG: 3-Conductor
	ED ITEMS	
	0200001362 0300007229 0400001719 0400007666 1505348E01 3100120365 4210217A02 4210217A02 4282387D05	NUT, 6-32 x 1/4" x 3/32" SCREW, 6-32 x 3/8 WASHER, Flat LOCKWASHER #6 COVER, Bottom STRIP, Terminal STRAP, Cable Harness CLIP, Cable (Nylon) CLAMP, Cable

NLN4607A Tone-Only, Fast Timing, Option PLF-1182-0

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R19 R20 R27	0600124A89 0600124B16 0600124A93	RESISTOR, Fixed: n±10% 47k±5%; 1/4W 560k±5%; 1/4W 68k±5%; 1/4W

REVISIONS

BOARD AND SUFFIX NO.	REFERENCE SYMBOL	CHANGE
NLN4486A	C19	Was 2182428B1802 uF
NLN4478A	R34	Was 0600124C17, 47 A
NLN4514A		
NLN4486A-1	C19	Changed to 2182428B62, .01 uF
NLN4478A-1	R34	Changed to 0600124C45, 680 a
NLN4514A-1	1	
NLN4486A-2	C37	Added
NLN4478A-2	Q10	Added
NLN4514A-2	R87	Added
	CRI	Deleted, was 4883654H01

52 PARTS LISTS



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_ First Fold	DIAGRAMS (indicate diagram number/description)	First _ Fold
	Are adequate	· old
	Are too small too big	
	Should contain the following additional information:	
	Contain the following errors:	
	PARTS LISTS	
	Are adequate	
	The following information is incorrect or should be added:	
	I prefer exploded views for parts identification	
Second	THEORY/TROUBLESHOOTING INFORMATION	Second
Fold	I use troubleshooting charts frequently.	Fold
	I do not use troubleshooting charts.	
	I prefer tabular symptom/remedy charts.	
	The following information should be added (or corrected):	
	MODEL CHARTS	
	I use charts to determine if manual is applicable to my radio model.	
	I use the charts to determine content of model or identify what chassis/kits are in the model; or:	
	I do not use these charts.	

PRINTED CIRCUIT BOARD DETAILS
I use printed circuit details for component location only.
In addition to component location, I use printed circuit details for:
I prefer photographs/drawings with call-outs for component location purposes.
Different shades of gray are adequate for double-sided boards.
I prefer use of different colors for double-sided boards.
CONDENSED SERVICE BOOKLET/SHEET
(With mailer card for ordering the companion Theory/Troubleshooting manual)
1. Are useful service tools
2. Should also include
3. Response time to mailer card requests for companion theory/troubleshootin
manual is: OK Too Long (DAYS)
OTHER COMMENTS
My name is
Company
Address
City State Zip
Phone no. (include area code)
No Postage Stamp Necessary if Mailed in the United States Postage Will Be Paid by Addressee
BUSINESS REPLY MAIL First Class Permit No. 75 Ft. Lauderdale, FL
First Class Permit No. 75 Ft. Lauderdale, FL
MOTOROLA, INC. 8000 W. Sunrise Blvd.
Ft. Lauderdale, Florida 33322

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MOTOROLA PAGING ENCODERS

"Moden" 100
"Moden" 36
Alert Central



"Moden" 100 Paging Encoder



"Moden" 36 Paging Encoder



Alert Central Paging Encoder



MOTOROLA INC.

Communications Division

ENGINEERING PUBLICATIONS

8000 WEST SUNRISE BOULEVARD

FT. LAUDERDALE, FLORIDA 33322

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PERFORMANCE SPECIFICATIONS

PAGING ENCODER MODEL	''Moden'' 100	''Moden'' 36	Alert Central			
CODE CAPACITY	90 Individual 10 Group	30 Individual 6 Group	5 Individual 1 Group			
FREQUENCY STABILITY	±.15% from 0°C to +50°C (25°C Reference)					
TONE OUTPUT	Adjustable to +2 dBm maximum @ 300 Hz with less than 3% distortion into 600 ohm load; ±2 of 6 dB/Octave de-emphasis from 300 to 3000 Hz, reference 1000 Hz.					
TONE FREQUENCY RESPONSE (WITHOUT DE-EMPHASIS, C30 REMOVED)	±3 dB @ 300-3000 Hz, reference 1000 Hz ±1 dB @ 67-202 Hz, reference 1000 Hz					
TONE A PULSE TONE B PULSE	See "Tone Coding" Section					
POWER: AC	117 Vac ±15% @ 60 Hz or 234 Vac ±15% @ 50 Hz less than 10 watts of operation					
DC	12 to 18 V dc 250 mA maximum operating current @ 18 V dc					
DIMENSIONS	9"D x 7"W x 1.85"H (22.86 cm D x 17.78 cm W x 4.699 cm H)					
WEIGHT	2.5 pounds (1.125 kg)					

SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

MODEL CHART

CODE: 1,2 = NUMBER OF ITEMS SUPPLIED O = ITEM OMITTED OR DELETED		DESCRIPTION "MODEN" 100 PAGING ENCODER "MODEN" 36 PAGING ENCODER ALERT CENTRAL PAGING ENCODER		BASE & 230 V TRANSFORMER, "MODEN" 100 BASE & 230 V TRANSFORMER, "MODEN" 36 BASE & 230 V TRANSFORMER, ALERT CENTRAL SUBAUDIBLE KIT (LOCAL) TONE-ONLY, BATTERY SAVER TONE-ONLY, FAST TIMING FIXED TONE A (ALERT CENTRAL ONLY)	"MODEN" 100 READ-ONLY MEMORY KIT "MODEN" 36 & ALERT CENTRAL READ-ONLY MEMORY KIT
ITEM	DESCRIPTION	MODEL	E08ENC0100AL E08ENC0036AL E08ENC0006AL	OPTIONS R165AB R165AA R165AC R166AA R167AA R167AA R177AA	FIELD OPTIONS NLN1442A NLN1435A
					422
NLN1434A	115 V BASE ASSEMBLY	<u> </u>	1		
NLN1440A	230 V BASE ASSEMBLY			1	
NLN4488A	DISPLAY READOUT		1		
NLN4487A	TOP COVER AND KEYBOARD		1		
NLN1433A	115 V BASE ASSEMBLY		1	0	ن کو کا کا کا د
NLN1439A	230 V BASE ASSEMBLY			1	
NLN4481A	DISPLAY READOUT		1		
NLN4480A	TOP COVER AND KEYBOARD		1		
NLN1438A	115 V BASE ASSEMBLY		1	0	
NLN1441A	230 V BASE ASSEMBLY			1	
NLN4415A	DISPLAY READOUT		1		
NLN4483A	TOP COVER AND KEYBOARD		1		
HUNTEDA	TOT COVER THE RETBOARD		1		
NTT NT4402 A	DEAD ONLY MEMORY CODE DI AN		2 1 1		
NLN4482A	READ-ONLY MEMORY CODE PLAN		2 1 1		2 1
NLN4534A	CODE LABEL		1 1 1		1 1
NLN4533A	SERIAL LABEL		1 1 1		
	CURLINOTER BY OCH THE				
NLN4484A	SUBAUDIBLE LOCAL KIT			1	
NLN4485A	BATTERY SAVER TONE-ONLY KIT			1	
NLN4607A	FAST TIMING TONE-ONLY KIT			1	
	FIXED TONE A (ALERT CENTRAL ONLY)		1	1	

EPF-7505-O

DESCRIPTION

1. INTRODUCTION

The "Moden" Series Paging Encoders are the principal control units for small to medium size radio paging systems. The paging system provides radio contact with a selected individual or group of individuals. A typical paging system consists of a paging encoder, which contains tone generating and control equipment, a microphone for voice messages, a radio transmitter installation (base station), and pocket-size paging receivers (tone-only or tone-and-voice).

Selective radio paging is accomplished by transmitting an rf carrier which is frequency modulated by a series of audio tones, and in some cases by a voice message. Each paging recipient carries a pocket receiver that responds to a particular sequence of the audio tones. The receiver remains muted until the proper tones are received, after which an audible alert tone is produced. In the case of a tone-only page, this alert tone is a signal for the paged person to perform some prearranged action, such as calling a telephone number or reporting to a specific location. For a tone-and-voice page, the alerting tone is followed by a voice message of variable length.

The "Moden" Series Paging Encoders includes three different models. The "Moden" 100, the "Moden" 36, and the Alert Central paging encoder versions differ in their call code capacity. The "Moden" 100 paging encoder has a call code capacity of 90 individual codes and 10 group codes. The "Moden" 36 paging encoder has a call code capacity of 30 individual codes and 6 group codes. The Alert Central paging encoder has a call code capacity of 5 individual codes and 1 group code.

2. PHYSICAL DESCRIPTION

The basic paging encoder is housed in a self-contained desk-top console, which includes an integral pushbutton keyboard and display. All circuit boards and components are packaged in the same desk-top unit with the keyboard and display.

The keyboard is different for each of the three models. The "Moden" 100 paging encoder has 12 pushbuttons: 0 through 9, P (page), and T (talk). The "Moden" 36 paging encoder has eight pushbuttons: 0 through 5, P (page), and

T (talk). The Alert Central paging encoder has eight pushbuttons: 1 through 5, P (page), T (talk), and a red pushbutton for group calls.

The display is also different for each of the three models. The "Moden" 100 paging encoder has a PAGE lamp, a TALK lamp, and two LED displays for a two-digit call code number. The "Moden" 36 paging encoder has a PAGE lamp and two LED displays for a two-digit call code. The Alert Central paging encoder has a PAGE lamp and a LED display for a single-digit call code.

3. ACCESSORIES

Several accessories may be used with the paging encoders. The accessories are required either to complete the radio paging system, or to modify existing equipment for compatibility with a radio paging system. These items are required in addition to the base station and paging receivers.

a. TKN6065B Cable Kit

This cable kit is required when the paging encoder is used with a consolette base station (local control), a "Compa-Station" base station (local and extended local control), or a remote control console. The kit consists of an 8-foot, 6-conductor vinyl covered cable. Spade lugs terminate both ends of the cable for connection to the encoder and the appropriate control unit or base station. The cable kit can also be used to parallel two encoders for increased capacity.

b. TKN6067A Cable Kit

This cable kit is required when the paging encoder is used with a PT Series "Handie-Talkie" Radio. The kit consists of an 8-foot, 5-conductor vinyl covered cable. One end of the cable is terminated in spade lugs. These spade lugs are connected to the terminal boards on the back of the encoder. The other end of the cable is terminated in a 4-pin plug which mates with the microphone input receptacle on the PT Series "Handie-Talkie" Radio.

c. "Private-Line" Control Kit

When the paging encoder is used with a "Private-Line" base station, a "Private-Line" Control Kit is required in the base station. The

purpose of the control kit is to remove "Private-Line" tone modulation from the transmitter when paging tones from the encoder are being transmitted.

d. Microphones

Voice messages originate from the TMN1005A Desk Microphone for local control PL systems, while the TMN1004A is normally used for standard squelch applications.

4. OPTIONS

As indicated in the "Model Chart," several factory-installed options are available for use with the paging encoder. The choice of the option(s) depends on the system configuration (subaudible paging, remote control, "Private-Line" squelch, etc.). These options are described in the following paragraphs.

a. Delete 115 VAC and Add 230 VAC Option

This option enables the "Moden" Series Paging Encoders to be adapted to a 230-volt power source.

b. Subaudible Paging (Local)

When the paging encoder is to be used in a system with subaudible coding, the NLN1130A Subaudible Interface Kit is required. This kit is installed in the associated base station (local control "Private-Line" base station with "PL" tone reed removed) and interconnected as shown in Figure 13. Separate instructions are supplied with the interface kit.

NOTE

Two-tone standard and subaudible codes cannot be mixed on the same encoder. To intermix these signaling schemes within the same system requires two separate encoders.

c. Tone-Only Option with Battery Saver

This option determines the tone timing and jumper configuration on the paging encoder for paging tone-only pagers with battery saver.

d. Tone-Only, Fast Timing Option

This option determines the tone timing and configuration of the paging encoder for fast timing, tone-only paging (see "Tone Coding" section, Figure 1).

e. Fixed Tone A Option (Alert Central Paging Encoder Models Only)

This option changes the Alert Central paging encoder from a fixed tone B frequency to a fixed tone A frequency. With this option, the Alert Central paging encoder output frequency consists of a fixed tone A frequency, while the tone B frequency depends on the digit entered with the keyboard.

5. FIELD OPTIONS

As indicated in the "Model Chart," field options are available for use with the paging encoder. The choice of the option(s) depends on the paging encoder used. These options are described in the following paragraphs.

a. "Moden" 100 Paging Encoder Read-Only Memory Kit, NLN1442A

This kit consists of four read-only memories (ROM) and a coding label. The four ROMs are labeled with a reference designation (U22, U26, U28, U30) and a tone group number. The coding label, which is to be affixed to the underneath surface of the paging encoder, designates the tone group used. For nonstandard tone groups, the coding label designates the frequency for each keyboard pushbutton.

b. "Moden" 36 and Alert Central Paging Encoder Read-Only Memory Kit, NLN1435A

This kit consists of two read-only memories (ROM) and a coding label. The two ROMs are labeled with a reference designation (U22, U28) and a tone group number. The coding label, which is affixed to the underneath surface of the paging encoder, designates the tone group used. For nonstandard tone groups, the coding label designates the frequency for each keyboard push-button.

6. FEATURES

Several features are available for use with the paging encoder. These features are described in the following paragraphs.

a. Alert Central Two-Step Paging Operation

The standard paging operation of the Alert Central paging encoder consists of one step; when any of the numbered keyboard pushbuttons or the red keyboard pushbutton is depressed, the associated paging tone is automatically sent to the base station. Two-step paging operation consists of depressing one of the numbered pushbuttons, and then depressing the page (P) keyboard pushbutton to initiate the paging tones.

To adapt the Alert Central paging encoder to two-step paging operation, remove jumper JU9, and then reinsert the keyboard plug (P1) black wire (tied back) into position eight on plug P1.

b. Remote Subaudible Paging

By specifying tone groups 17x8, 18x8, and 19x8 as the tone groups used, the paging encoder will generate subaudible frequencies at eight times the rate. These tone groups in conjunction with a remote control console allow use of stan-

dard voice grade lines for subaudible paging. At the base station, an SP57011801 Subaudible Remote (Divide by Eight) Kit is necessary to divide the paging tones by eight and provide the interface to the base station for transmission. The base station must be equipped with PL operation (refer to Figure 14).

c. Nonstandard Tone Groups

Paging tones, other than the standard tone groups listed in the "Tone Coding" section, can be generated by the paging encoder. The limiting factors are as follows: subaudible tones should not be mixed with audible tones, and the number of frequencies should correspond to the capacity of the paging encoder ("Moden" 100 paging encoder has ten frequencies and "Moden" 36 and Alert Central paging encoders have six frequencies).

TONE CODING

1. INTRODUCTION

Motorola radio paging systems employing the "Moden" 100, "Moden" 36, and Alert Central Paging Encoders use two-tone sequential signaling (refer to Figure 1). Two discrete audio tones (tone A and tone B) are transmitted for a specific period of time. Each pager in the system responds to a unique combination of tones, which is determined by filters installed in the pager. The types of paging calls that may be generated by the paging encoder are determined by the coding type circuits and the programming of tones into the tone synthesizer circuitry of the paging encoder. These functions are implemented mainly by special read-only memories (ROMs) which are programmed according to a desired code plan or code type for the paging encoder.

2. CODE PLAN DESCRIPTION

There are a number of different code plans used in paging systems. Each code plan has a letter designator that defines the code plan and its associated tone groups (refer to Table 1). Each tone group contains ten frequencies (refer to Tables 2 through 21). Tables 2 through 21 show the correlation between tone group's tone number, keyboard number, frequency, and ROM output bits. Through the use of Tables 1 through 21 and the pager code (cap code), the frequencies of the two audio selective elements used in the pager decoding circuit can be determined.

Table 1.

Code Plan Designator and Tone Group Used

CODE PLAN DESIGNATOR	тот	NE GROUP U	ISED
В	1	2	3
С	1	2	4
D	1	2	5
E	1	2	6
F	1	3	4
G	1	3	5
H	1	3	6
J	1	4	5
K	1	4	6
L	1	5	6
M	2	3	4
N	2	3	5
P	2	3	6
Q	2	4	5
R	2	4	6
S	2	5	6
Т	3	4	5
U	3	4	6
V	3	5	6
W	4	5	6
Y	A(QC)	B(QC)	Z(QC)
AZ	17	18	19
8AZ	17×8	18 x 8	19×8
GE	A(GE)	B(GE)	C(GE)

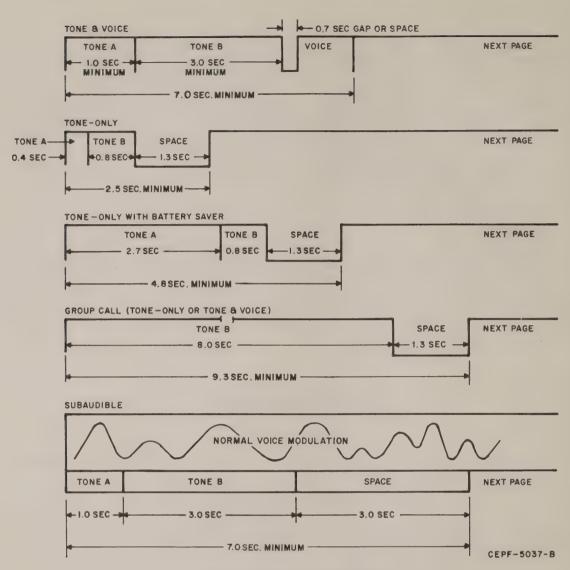
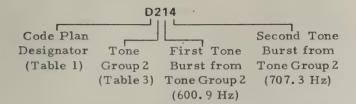


Figure 1. Two-Tone Signaling Options

a. Paging Code Plans

The code plans used in the paging system are shown in Table 1. The code plan letter designator is listed in the left-hand column of the table (B through GE). The numbers listed to the right of the code plan designator indicate the tone groups available for that code plan. These paging encoders are programmed for one tone group out of a code plan. For example, a paging encoder using code plan C will be programmed for either tone group 1, 2, or 4; for code plan AZ, a paging encoder will be programmed for either tone group 17, 18, or 19. Code plan Y is used for "Quik-Call" systems. Code plans AZ and 8AZ are used for subaudible systems. Code plan GE is used for General Electric Co. paging systems.

In paging systems, a call code consists of a letter prefix and a three-digit number. letter prefix designates the code plan or code type. The most significant digit is used to determine from which tone group that the first and second tone burst tones are selected. For example, assume a system operating in code plan D which indicates that tone groups 1, 2, or 5 are used (shown in Table 1). Next, assume that the pager to be paged has a cap code of D214. The most significant digit is 2 which means that the first tone and the second tone will be a tone from tone group 2. The second and third digits of the call code determine the tone number selected from the tone group. The second digit, number 1, indicates the first tone to be tone number 1 of tone group 2 (600.9 Hz). See Table 3. The third digit, number 4, indicates the second tone to be tone number 4 of tone group 2 (707.3 Hz).



Refer to any one of Tables 2 through 21; notice the correlation between the tone number column and the keyboard numbers of the "Moden" 100, "Moden" 36, and Alert Central paging encoders. For the preceding example (D214), keyboard pushbuttons 1 and 4 are used to page pager code D214 when using the "Moden" 100, "Moden" 36, or Alert Central paging encoders.

b. Tone Groups

NOTE

The Alert Central paging encoder red keyboard pushbutton is equivalent to keyboard zero on the "Moden" 100 and "Moden" 36 paging encoders.

For "Moden" 36 and Alert Central paging encoders, the tone groups are broken into upper and lower tone groups. The upper tone group consists of tone numbers zero through five (0, 1, 2, 3, 4, 5), and the lower tone group consists of tone numbers five through nine and zero (5, 6, 7, 8, 9, 0). The first six tone numbers (0 through 5) and the keyboard numbers are the same except as previously noted for the alert central red keyboard pushbutton. The relationship between the lower tone group tone numbers (5 through 9 and 0) and the keyboard numbers are different in comparing the "Moden" 100 to the "Moden" 36 and Alert Central paging encoders. Tone number five is translated into keyboard zero on the "Moden" 36 and into the red keyboard pushbutton on the Alert Central. Tone numbers 6, 7, 8, 9, and 0 correspond to keyboard numbers 1, 2, 3, 4, and 5 on both the "Moden" 36 and Alert Central paging encoders. In Alert Central paging encoder models, the fixed or common tone is the frequency corresponding to keyboard zero in Tables 2 through 21 or position zero on the label located on the bottom of the unit.

c. Subaudible Tone Coding

Subaudible coding provides the facility for simultaneous transmission of paging calls and voice communications on the same channel. Low frequency paging tones from 67.0 to 202.7 Hz at a low carrier deviation of 0.5 to 1 kHz are used so that no audible response will be produced in co-channel receivers engaged in audio communications.

Subaudible paging codes differ from the standard paging codes due to the low frequency required. The subaudible tone groups are designated groups 17, 18, 19, 17x8, 18x8, and 19x8 in Tables 10 through 15. Determination of frequencies is identical to that described in the preceding paragraph.

d. Group Call Coding

Pagers with the group call option are assigned two code numbers: one for individual call and one for group call. If the individual number is used to call a group pager, it alone will be alerted as is the standard pager. If the group call number is used, all other pagers in the same group will be alerted along with this pager.

Group call is accomplished by transmitting a single continuous tone for approximately eight seconds. This tone will alert all group call pagers that use this tone frequency in the tone B position.

An example of a pager code with group call is as follows: D567/177, where 177 is the group call number. The first digit gives the tone group and the second and third digits correspond to the tone number; therefore, 177 means tone number? from tone group 1. According to Table 2, the group call tone for this pager is 483, 5 Hz.

The maximum number of pagers that may be included in a group is equal to the total number of paging tones available in the paging encoder, minus one. The maximum number of groups in a system is equal to the number of paging tones available.

e. Tone Timing

The different timings associated with various two-tone signaling options are shown in Figure 1. To implement these different timings, resistor values are changed at certain parts of the paging encoder circuitry, which is explained in the "Setup Procedures" paragraph in the "Installation" section of this manual.

Table 2. Tone Group 1, 1U, and 1L Frequencies and ROM Outputs

TORIL	KEYBOAF	KEYBOARD NUMBER		CDEO					Œ	EAD-C	READ-ONLY MEMORY OUTRUT BITS	MEMO	RY 0	UTPU	F BITS					
	"MODEN"	& ALERT CENTRAL	25 T J	(Hz)	215	214	213	212	211	210	29	28	27	26	25	24	23	22 2	21	20
11	0	(0		330.5	0	0	1	1	0	0	1	1	0	0	0	0	0	1	0	-
	-			349.0	0	0	1	-	0	-1	0	0	1	0	0	1	0	0	0	0
	2	2 UPPER	E E	368.5	0	0	1	1	0	1	1	0	1	0	0	0	0	1	0	_
	8	3 / TONES	ES	389.0	0	0	-	-	-	0	0	0	-	0	0	1	0	0	0	0
	4	4	L	410.8	0	1	0	0	0	0	0	-	0	0	0	0	1	0	0	0
	5	5	0	433.7	0	1	0	0	0	0	-	-	0	0	_	-	0		-	_
	9		-	457.9	0	П	0	0	0	1	0	-	0	-	1		1	0	0	
	7	IOWFR	2	483.5	0		0	0	1	0	0	0	0	0	1	1	0	1	0	_
	œ	TONES	3	510.5	0	-	0	-	0	0	0	1	0	0	0	0	0	П	0	
	6		4	539.0	0	-	0	-	0	0	1		1	0	0	1	0	0	0	0
	0		25	330.5	0	0	-	-	0	0	-	1	0	0	0	0	0	-	0	_
1		The state of the s																		

Table 3. Tone Group 2, 2U, and 2L Frequencies and ROM Outputs

	-					-						
	20		-	-	-	-	0	-		0	-	-
	21	0	0	0	0	-	0	0	0	0	0	0
	22	0	0	1	0	0	0	1	1	0	0	0
	23	0	_	0	1	0	1	0	0	0	0	0
S	24	-	0	0	1	pI	0	0	0	1	0	1
TBIT	25	0	0	0	0	1	1	0	1	0	0	0
UTPU	26	0	0	1	0	П	1	0	0	0	0	0
ORY O	27	-	0	0	-	0	0	1	0	1	-	1
MEMC	28	0	0	1	0	0	0	0	-		0	0
NLY	29	-	0	1	1	0	0	0		-	-	1
READ-ONLY MEMORY OUTPUT BITS	210	1	0	0	1	0	1	0	0	1	0	1
æ	211	0	0	0	0	0	0	П	0	0	0	0
	212	1	0	0	0			1	0	0		-
	213	0		П		_	1	-	0	0	0	0
	214	1	1	1		1	1	1	0	0	0	П
	215	0	0	0	0	0	0	0	-		-	0
FREO	(Hz)	569.1	6.009	634.5	6.699	707.3	746.8	788.5	832.5	879.0	928.1	569.1
g				Œ	S		0	-	2	3	4	ر ب
WOODEN" 38	& ALERT CENTRAL			UPPER	TONES]	OWFR	TONES		
UN ON	880	0	-	2	3	4	57		C	2		
KEYBOARD NUMBER	"MODEN" 100	0	-	2	n	4	ນ	9	7	80	6	0
TONE	NUMBER	0	-	2	8	4	5	9	7	80	6	0
	"						4	1	_	25		>
TONE	GROUPS	4			2 -		-					
I	GR							L.				
							4					

Table 4. Tone Group 3, 3U, and 3L Frequencies and ROM Outputs

11407		KEYBOAF	KEYBOARD NUMBER		EDEO					-	READ-ONLY MEMORY OUTPUT BITS	SNLY	MEM	DRY O	UTPU	TBIT	S				
NUMBER "MODEN"	100 100	EN	& ALERT CENTRAL	36 L	(Hz)	215	214	213	212	211	210	29	28	27	26	26	24	23	22	21	20
0 0	0		(0		1092.4	-	-	0	-	0	0	0	0	-	0	0	-	0	0	П	0
pred	pro-d		1		288.5	0	0	-	0	1	0	0	0	-	0	0	0	0	П	0	1
2 2			2 UPPER	E E	296.5	0	0		0	1	0	0	7	0	1	1	0	0	1	0	1
n	(-7	3	3 TONES	ES	304.7	0	0	-	heed	0	0	0	0	0	-	0	0	0	-	1	1
4	Ì	4	4		313.0	0	0	-	1	0	0	0	-	0	0	1	1	0	0	0	0
2		5	5	0	953.7	1	0	0	1	0	1	0	-	0	0	-		0	-	-	1
9		9		-	9.626	_	0	0	-	0	1	1	-	1	0	0	-	-	0	0	-
7		7	LOWER	2	1006.9	1	1	0	1	0	0	0	0	0	0	0	0	0	-	-	0
80		8	TONES	3	1034.7	1	1	0	П	0	0	0	0	0	0	1	1	0	-1	0	0
6		6		4	1063.2	1	1	0	7	0	0	0	0	0	1	1	0	0	-	0	0
0		0		22	1092.4	-	-	0	H	0	0	-	0	-	0	0	1	0	0	1	0
	-																				

Table 5. Tone Group 4, 4U, and 4L Frequencies and ROM Outputs

MODEN" RALENT (Hz) 215 100 CENTRAL (Hz) 215 215	TONE	EYBOAR	KEYBOARD NUMBER	R 26	FREG					R	AD-0	NLY	READ-ONLY MEMORY OUTPUT BITS	N ON	TPUT	BITS					
0 0 321.7 0 1 1 339.6 0 2 2 UPPER 358.6 0 3 3 3 TONES 378.6 0		00 00	& ALE CENTF	RT	(Hz)	215	214	213	212	211	210	29	28	27 2	26	25 2	24 2	23 2	22 2	21 2	20
1 1 2 339.6 0 1 2 2 UPPER 358.6 0 1 2 3 3 3 4 4 399.8 0		0	0		321.7	0	0	-	-	0	0	-	0	0	0	0		0			
2 2 UPPER 358.6 0 3 3 TONES 378.6 0 4 4 399.8 0					339.6	0	0	1	-	0	0			1	0	0	1	0	-		0
3 3 TONES 378,6 0		2	^	PER	358.6	0	0	1	П	0	-	0	-	-	0	0	0	0			0
4 4 399.8 0		3		NES	378.6	0	0	1	1	0	-	-	-	real	0	0	0	0		-	0
		4	4		399.8	0	0	1	-	-	0	0		-	0	0	-	-	0	0	0
4 V A 5 5 5 (0 422.1 0 1		5	5	0	422.1	0	-	0	0	0	0	-	0	0	0	1	0	0	0	0	
6 6 1 445.7 0 1		9			445.7	0		0	0	0	1	0	0	0	-	0		0			
7 7 LOWER 2 470.5 0		7	LOWER	_	470.5	0	1	0	0	0		-		0	0	0	0	0		0	
3 496.8 0		∞	TONES		496.8	0	-	0	0	-	0	0	-	0		1	0	-	0	0	0
9 9 4 524.6 0 1		6		4	524.6	0	1	0	-	0	0	-	0	0		0	0	0		-	0
v v 0 0 (5 321.7 0 C		0		2	321.7	0	0	-	-	0	0	1	0	0	0	0	-	0			

Table 6. Tone Group 5, 5U, and 5L Frequencies and ROM Outputs

GROUPS NUMBER "MODEN" RALERT CENTRAL CENTRAL CENTRAL 100 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	TONE	11	TONE	KEYBOAF	KEYBOARD NUMBER	36	FREO					R	EAD-C	NILY	MEMC	RYO	UTPU	READ-ONLY MEMORY OUTPUT BITS	10				
1	GROUI	PS	NUMBER	"MODEN" 100	& ALER CENTRA	J	(Hz)	215	214	213	212	211	210	28	28	27	26	25	24	23	22	21	20
5U	*		0	0	0		553.9	0	-	0	П	0	-	0		0	0		П	1	0	0	-
5U 2 UPPER 617.4 0 1 1 0 0 0 0 0 1 1 0 0 0 0 0 1 1 0 0 0 1 1 0 0 1 0 0 1 0 0 0 1 0 0 0 1 0				-			584.8	0	1	0	1	1	0	0	0	0	-	0	0	1	0	0	0
For the second section of the second section of the second section sec	20		2	2		8	617.4	0	1	1	0	0	0	0	1	.0	1	1	1	0	П	0	0
A	3		m	67)		ES	651.9	0	7	1	0	0	1	0	П	0	0	0	1	1	0	0	7
For the second s			4	4	4		688.3	0	1	1	0	1	0	0	0	1	0	0	0	0	0	1	-
6 6 6 1 1 767.4 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 0 1	2	4	5	5	5	0	726.8	0	-	-	-	0	0		0	0		1	0	1	0	0	0
7 7 LOWER 2 810,2 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			9	9		-	767.4	0	-	-	-	0		1	0	0	-	1	-	0	-	0	0
8 8 TONES 3 855.5 1 0 0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1		- ū	7	2	LOWER	2	810.2	1	0	0	0	0	0	0		0	0	0	0	0	0	-	0
9 4 903,2 1 0 0 1 0 0 0 0 0 1		7 –	8	œ	TONES	3	55.	1	0	0	0	0	1	0	1	0	1	0	П	0	-	0	-
0 (5 553.9 0 1 0 1 0 1 0 1 0 0 1 1			6	6		4	903.2	1	0	0	-	0	0	0	0	0	0	1	-	0	0	-	0
	->	->-	0	0		2	553.9	0	1	0		0	1	0	1	0	0	7	1		0	0	-

Table 7. Tone Group 6, 6U, and 6L Frequencies and ROM Outputs

				KEYBOAF	KEYBOARD NUMBER							8	READ-ONLY MEMORY OUTPUT BITS	NLYA	1EMO!	RY OL	TPUT	BITS					
9	GROUPS	S	NUMBER	"MODEN"	"MODEN" 36 & ALERT	7.36	(Hz)	216	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20
					2518111	1																	
-	4		0	0	6		1122.5	1	1	0	-	0	0	0	-	0	0		0	0	0		0
				-	-		1153.4	-	-	0	-	0	0	0	-	0		0	-	0	-	0	0
	- 3		2	2	2 UPP	UPPER	1185.2	-	-	0	7	0	0	0	1		0	0	0	0	7	-	0
	3 -		3	3	3 TONES	ZES	1217.8	1	1	0	1	0	0	-	0	0	0	0	-	1	0	0	0
_			4	4	4		1251.4	1	1	0	1	0	0	1	0	0	-	0	1	0	0	-	0
9	>	4	5	5	5	0	1285.8	1	1	0	1	0	0	1	0	1	0	0	0	0	-	-	0
			9	9		-	1321.2	-	-	0	-	0	0	-	-	0	0	-	0	0	0	-	0
		- 5	7	~	LOWER	2	1357.6	1	-	0	1	0	0	-	1	0	П	0	-	7	0	0	0
		J -	∞	8	TONES	3	1395.0	-	1	0	-	0	0	1	1	7	0	0	-	0	-	-	0
			6	6		4	1433.4	1	1	0	-	0	1	0	0	0	0	-	-	0	-	0	0
>		->	0	0		22	1122.5	-	-	0	-	0	0	0	-	0	0		0	0	0	-	0

Table 8. Tone Group 10, 10U, and 10L Frequencies and ROM Outputs

10L >					KEYBOA	KEYBOARD NUMBER	ER						a	EAD.C	> IN	MEMO	RY O	ITPII	T RITS	-				
NUMBER N		TONE		TONE	"HADDDEN!"	"MODE	٧٠, 36	FREG		-												ı	1	
10U 2 2 2 UPPER 1555.2 1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 0 0 0 1 1 0 1 0 0 0 0 1 0	9	ROUP	S	NUMBER	100 100	& AL CENT	ERT	(Hz)	216	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20
10U 2 2 2 2 OVPER 1555.2 1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	4	4		0	0	(0		1472.9	-	1	0	1	0	-	0	0	0		-	-	0	0	-	0
10U 3 3 3 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4				-	1	-			H	1	0	-	0	-	0	-1	0	0	0	-	0	-	0	0
		100		2	2		PPER	1555.2	1	-	0	1	0	1	0	-	0	-	0	-	0	-		0
4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 1642.0 1 1 0 1 1 1 0 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 0 1 1 0 0 1 0 1 1 0 1 1 0 1 1 0 1 1 0 <th></th> <th></th> <th></th> <td>3</td> <td>3</td> <td></td> <th>SHOO</th> <td>1598.0</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>-</td> <td>0</td> <td>0</td> <td></td> <td>-</td> <td>0</td> <td>0</td> <td>0</td>				3	3		SHOO	1598.0	1	1	0	1	0	1	0	1	-	0	0		-	0	0	0
10				4	4	4		1642.0	1	1	0	1	0		1	0	0	1	0	0	0	0	-	0
6 6 6 1 1733.7 1 1 1 0 1 1 1 1 1 1 0 0 1 1 1 1 0 0 1 1 1 0	10	>	4	5	5	5	0		1	1	0	-	0	1	-	0	-	0	0	0	-			0
7 7 LOWER 8 2 1781.5 1 1 0 1 1 1 1 0 <t< th=""><th></th><th></th><th></th><th>9</th><th>9</th><th></th><th>-</th><th>1733.7</th><th>1</th><th>1</th><th>0</th><th>-</th><th>0</th><th>П</th><th>-</th><th>1</th><th>0</th><th>0</th><th>1</th><th>1</th><th>0</th><th>1</th><th>0</th><th>0</th></t<>				9	9		-	1733.7	1	1	0	-	0	П	-	1	0	0	1	1	0	1	0	0
8 8 TONES 3 1830.5 1 1 0 1 1 0 0 0 0 0 0 1 1 0 0 0 0 0 0			- ;	2	2	LOWER		1781.5	1	1	0		0	-1	-	-	-	0	0	0	0	0		0
9 4 1881.0 1 1 0 1 1 0 <th></th> <th></th> <th>10L</th> <th>8</th> <th>œ</th> <th>TONES</th> <th></th> <th></th> <th>1</th> <th>7</th> <th>0</th> <th>1</th> <th>1</th> <th>0</th> <th>0</th> <th>0</th> <th>0</th> <th>0</th> <th>1</th> <th>1</th> <th>0</th> <th>0</th> <th>0</th> <th>0</th>			10L	8	œ	TONES			1	7	0	1	1	0	0	0	0	0	1	1	0	0	0	0
0 5 1472.9 1 1 0 1 0 1 0 0 0 0 0 0				6	6		4	1881.0	1	1	0	1	-	0	0	0	1	0	0	0	0	0	-	0
	->		->	0	0		2	1472.9	1	-	0		0	1	0	0	0	1	-	-	0	0	1	0

Table 9. Tone Group 11, 11U, and 11L Frequencies and ROM Outputs

				KEYBOAF	KEYBOARD NUMBER	~						a	READ ONLY MEMORY CLITTERT	> IN	MEMO	0 / 0	ПОТІ	TRITE					
	TONE		TONE	WEST CONTRACTOR	"MODEN" 36	, 36	FREG							INC.	MEM			-				Ì	
5	GROUPS		NUMBER	100	& ALERT CENTRAL	3T AL	(Hz)	215	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20
4	4		0	0	0		1930.2	-	-	0	-	1	0	0		0	0	-		0	0	0	0
				-	pand		1989.0	-	1	0	1	1	0	0	1	П	0	0	-	0	0	0	0
	110		2	2	2 UPP	UPPER	2043.8	1	-	-	0	0	0	0	0.	0	-	0	0	0	7	0	0
			3	3	3 (TON	TONES	2094.5	1	-	-	0	0	0	0	6	p4	0	0	-	0	-	0	0
			4	4	4		2155.6	-		-	0	0	0	0	, _—	0		0	П	0		-	0
1	>	4	5	2	5	0	2212.2	1	1	1	0	0	0	1	o,	0	0	0	-	0	0	-	0
			9	9		-	2271.7	-	7	7	0	0	0	p—4	0	0				0	0	-	0
	*	- ;	7	7	LOWER	2	2334.6	-	-	-	0	0	0	-	7	0	0	1	1	0	-	0	0
	_		œ	00	TONES	3	2401.0	-	-	-	0	0	7	0	0	0	0	0	0	0	0	-	0
			6	6		4	2468.2	1	1	-	0	0	-	0	0	0	-	1	0	1	0	0	0
->		->	0	0		2	1930.2	1	-	0	-	-	0	0	П	0	0	-	-	0	0	0	0

Table 10. Tone Group 17, 17U, and 17L Frequencies and ROM Outputs

ITS	24 23 22 21 20	0 0 0 1 0	0 0 1 1 1	0 1 0 0 0	0 0 0 1 0	1 0 0 1 1	1 1 0 0 0	1 1 0 0 1	0 0 0 1 0	0 0 1 1 1	1 0 1 0 0	
3Y OUTPUT B	27 26 25	0 1 1	0 0 1	0 0 1	0 1 1	1 0 0	0 0 1	0 1 1	0 0 1	0 1 1	0 0 0	-
READ-ONLY MEMORY OUTPUT BITS	29 28	0	0 0	0 1	0 0	1 0	1 1	1 0	1 0	0 1	0	0
READ	212 211 210	1 0 1	0 0 0	1 1 0	1 1 0	0 0 1	1 0 1	1 0 1	1 0 1	1 0 1	1 0 1	-
	214 213	0 0	0 1	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	-
1	(Hz) 215	146.2 0	202.7 0	192.8 0	186.2 0	69.3 0	173.8 0	167.9 0	162.2 0	156.7 0	151.4 0	0
KEYBOARD NUMBER	"MODEN" 36 & ALERT CENTRAL	(0	-	2 UPPER	3 TONES	4	5) (0	1	LOWER 2	TONES \ 3	4	5
KEYBOA	"MODEN" 100	0	-	2	3	4	5	9	7	∞	6	0
	NUMBER	0	M	2	8	4	22	9	7	∞	6	0
	GROUPS	*		- 7	2 -		17 \$ 4	-		17.		,

Table 11. Tone Group 18, 18U, and 18L Frequencies and ROM Outputs

	TONE	ш	TONE	KEYBOAI "MODEN"	KEYBOARD NUMBER	100	FREQ					-	READ-ONLY MEMORY OUTPUT BITS	NLY	MEMO	RY OF	TPU	BITS				-	
	GROUPS	PS	NUMBER	100	& ALERT CENTRAL		(Hz)	216	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20
4	-		0	0	(0		103.5	0	0	0		0	0	0	0	0	0	-		0	-	0	
					-		141.3	0	0	0	-	0	1	0	0	0	0	0	-	0	0	-	
	180		2	2	2 UPPER	~	136.5	0	0	0		0	0		П	0	-		0	0	П	0	-
	-		8	3	3 TONES	·^	131.8	0	0	0		0	0	-	-	0	0	0	1	_	0	0	0
			4	4	4		127.3	0	0	0	1	0	0	-	0	0	7	1	_	0	0		-
00	>	4	5	5	5) (6	0	123.0	0	0	0	-	0	0	-	0	0	0	-	-	0	0	0	0
			9	9		_	74.4	0	0	0	0	0	poord			0	_	0	0	0	-	0	0
		- 5	7	2	LOWER	2	114.8	0	0	0	-	0	0	0		0		0	0	-	0	0	0
		<u></u>	00	∞	_	3	110.9	0	0	0	1	0	0	0	-	0	0	0	0		0	0	-
			6	6		4	107.2	0	0	0	-	0	0	0	0	0	-	1		0	0	-	0
->		->	0	0		۲,	103.5	0	0	0	1	0	0	0	0	0	0	1	П	0	1	0	

Table 12. Tone Group 19, 19U, and 19L Frequencies and ROM Outputs

		11001	KEYBOAF	KEYBOARD NUMBER	~						"	FAD.	BEAD-ON! V MEMORY OLITRITE BITS	MEM) Vac	ITDI	TOIL					
	TONE		"MODEN"	"MODEN" 36	, 36	FREQ							JAC I	INICINIC		0110	l Dil	0				
GROUPS NUMBER	NUMB	EB	100	& ALERT CENTRAL	3T AL	(Hz)	215	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20
0	0		0	0		67.0	0	0	0	0	0	1	p	0	0	-	-	-	0	0	0	0
proof	-		-	-		100.0	0	0	0	-	0	0	0	0	0	0	0	0	0	0	0	0
2	2		2	2 UPF	UPPER	79.7	0	0	0	0	0	1	1	r-d	-	0	0	-	0	-	1	1
<i>c</i> 0	60		3	3 (10	TONES	94.8	0	0	0	0	1	0	0	1	0		0	0	-	0	0	0
		4	4	4,		91.5	0	0	0	0	1	0	0	1	0	0	0	-	0	П	0	1
4		5	5	5	0	88.5	0	0	0	0	1	0	0	0	-	0	0	0	0	Н	.0	7
		9	9		-	85.4	0	0	0	0	-	0	0	0	0		0	-	0	-	0	0
		2	7	LOWER	2	82.5	0	0	0	0	7	0	0	0	0	0	7	0	0	-	0	-
	~		80	TONES	3	77.0	0	0	0	0	0	-	-	1	0	1	1		0	0	0	0
		6	6		4	71.9	0	0	0	0	0	,4	-1		0	0	0	-		0	0	-
>		0	0		22	67.0	0	0	0	0	0	-		0	0		-		0	0	0	0
										- Investor	-	- parameter	1	-		-	1					

Table 13. Tone Group 17 x (8), 17 x (8)U, and 17 x (8)L Frequencies and ROM Outputs

	21 20	0							0	1 0	0	
	22		0	0	-	_	-	0	-	0	0	
	23	0	0	0	0	C			0	0	0	_
ITS	24	0	0	-	0	_	0		H		-	C
READ-ONLY MEMORY DUTPUT BITS	25	-	0	0	0	C	0	0	0	0	-	-
DOT	26	0		0		0		0		0		0
MORY	27	0	0		0		0		0	0	0	0
Y ME	28	0		0	-1	-	-	0	0	0		0
ONL	29	-	0	0	0		-	П	1	-	0	-
READ	210			-	1	0	0	0	0	0	0	0
	211	0	0	0	0	0	0	0	0	0	0	0
	212		П		7		-	-	-		Н	
	213	0	0	0	0	0	0	0	0	0	0	0
	214	П	-	-	П	~		-	-	П	-	
	215	-		-	0	-	1	-	-	1		(
EDEO	(Hz)	1621.6	1542.4	1489.6	554.4	1390.4	1343.2	1297.6	1253.6	1211.2	1169.6	1621.6
NUMBER	& ALERT CENTRAL	0		2 UPPER	3 (TONES	4	5) (0	-	LOWER 2	TONES 3	4	22
KEYBOARD NUMBER	"MODEN" 100	0	parent.	2	٣	4	5	9	2	∞	6	0
TONE	NUMBER	0	-	2	3	4	5	9	7	8	6	0
TONE	GROUPS	4		17×	0		>		17×	7(8)F		>
		4					17 × (8)					->

Table 14. Tone Group $18 \times (8)$, $18 \times (8) U$, and $18 \times (8) L$ Frequencies and ROM Outputs

	20	0	0	0	0	0		0	0	0	0	0
	21	0	1	0	0	0		0	-		0	0
	22	0	0	П	0	0	-	-	0	-	0	0
	23	0	0	0	-	0	0	0	0	0	0	0
S	24	-	1	1	г	0	-	0	-		0	1
IT BIT	25	-	0	0	0	0	0	0	-	-	0	1
UTPU	26	0	0	П	0	1		0	-		0	0
ORY O	27	0	-	0	0	0	0	1	0	0	1	0
MEMC	28		0	0	0	0	-		0	-	0	1
NLY	29	0	0	0	0	0	0	0	0	0	-	0
READ-ONLY MEMORY OUTPUT BITS	210	0	0	0	0	0	0	0	0	-	0	0
H	211	0	0	0	0	П	-	0	1	0	0	0
	212		1	1	1		-	1	0	0	0	1
	213	0	0	0	0	0	0	0	0	0	0	0
	214	-	1	1	-	0	1	0	0	0	0	1
	215	-	-	1	1	7	0	1	1	1	П	1
1	(Hz)	1130.4	1092.0	1054.4	1018.4	984.0	595.7	918.4	887.2	857.6	828.0	1130.4
UMBER	"MODEN" 36 & ALERT CENTRAL			UPPER	TONES		0	1	LOWER 3	rones 3	4	2
3D N	2	0	-	2	3	4	ري '			-		
KEYBOARD NUMBER	"MODEN" 100	0	-	2	3	4	5	9	7	∞	6	0
1	NUMBER	0	r1	2	3	4	5	9	2	8	6	0
	10						4		_×	1(8)		->
	TONE	4		-8 -×	 ∩(8)		>					
	95	4					78 (8)					->
_		4										

Table 15. Tone Group $19 \times (8)$, $19 \times (8) U$, and $19 \times (8) L$. Frequencies and ROM Outputs

	20	0	0	0	0	0	0	0	0	0	0	0
	21	0	-	0	0	0		0	0		0	0
	22	0	-	-	0	0	0	0	0	0	0	0
	23	0	0	0	0	0	0	0	0	0	0	0
S	24	0	1	0	0	0	-	0	0	-	0	0
IT BIT	25	0	1	0	1	0	-	0	1	0	1	0
UTPU	26	0	1	0	0	0	0	0	1	-	1	0
JRY C	27	0	0	1	0	1	0	0	0	0	0	0
MEMO	28	0	-	7	1	0	0	0	1	-	1	0
NLY	29	0	П	0	П	0	0	-	0	-	1	0
READ-ONLY MEMORY OUTPUT BITS	210	0	0	-	0	0	0	-	0	-	0	0
R	211	0	0	0	0	0		0	0	0	0	0
	212	0	0	-	П	r-1	0	0	0		1	0
	213	0	1	-	1	г	-	-	1	0	0	0
	214	0	1	-	1	1	1	-	1	1	1	1
	215	-	0	0	0	0	0	0	0	0	Ó	7
FREQ	(Hz)	800.0	637.6	758.4	732.0	708.0	683.2	0.099	616.0	575.2	536.0	800.0
36	S			ER	IES		0	_	2	3	4	22
"MODEN"	& ALERT CENTRAL			UPPER	TONES				LOWER	TONES		
NO OK	ಶರ	0	1	7	3	4,	5		LO	10		
KEYBOARD NUMBER	"MODEN" 100	0	1	2	23	4	5	9	7	œ	6	0
TONE	NUMBER	0		2	87	4	5	9	7	80	6	0
	50						4			(8)L		-
TONE	GROUPS	~		-61 × 61	 ∩(8)		>					
	9	4					19 × (8)					->
		L	-									

Table 16. Tone Group A(QC), A(QC)U, and A(QC)L Frequencies and ROM Outputs

	-		1									1	
		20	-			0					0	0	
		21			-	10	-	-				0	0
		22	C	C		0		-	0	0	0	0	0
		23	-		0				0	0	0	0	1
	2	24		C)		-		0	-	0	0	0
F	211211	25		C	0	0	-		0	0	-	-	0
ITI	2012	26	0	0	0	0	C	0	0	0	0	0	0
Vac	on i	27		-	0	1	C	0	-	0	0	0	-
BACKA	IVICIVI	28	-	-	0	0	0	0	0	0	0	-	-
> 1MC	JINE T	29	0	0	0	0	0	0	-	0	П	0	0
BEAD ON! V MEMORY OUTER!	בעו	210	1	0	-	0		0	1	1	0	0	~
	1	211	0		0	1	0	0	0	0	0	0	0
		212	l i	-	0	0	1	0	0	1	0		-
		213	-	-	0	0	0		П	-	0	0	_
		214	0	0	1	1	1			-	0	0	0
		215	0	0	0	0	0	0	0	0	-	-	0
	FREQ	(Hz)	358.9	398.1	441.6	489.8	543.3	602.6	668.3	741.3	822.2	912.0	358.9
KEYBOARD NUMBER	"MODEN" 36	& ALERT CENTRAL	0		2 UPPER	3 (IONES	4	5) (0	-	LOWER 2	TONES 3	4	2
KEYBOAF	"MODEN"	100	0		2	m	4	2	9	7	<u></u>	6	0
TOME	ONE	NUMBER	0	-	2	3	4	5	9	7	∞	6	0
TOME	- ONE	GROUPS	4		A ()) D-		(ac) V A		Ą (SC)			>

Table 17. Tone Group B(QC), B(QC)U, and B(QC)L Frequencies and ROM Outputs

	1	Ţį.		1	1		1		1			
	20			-	0	-	-	0	0		-	
	21	c	0	0	0	-		0	0	0	0	0
	22	-	0	0	0	0	1	0	-	0	0	-
	23	0	0	0	0	0	0	-	0	0	0	0
SO.	24		0	1	-	0	-	-	-	1	0	-
JT BIT	25	0	-	1	П	-	-	0		0	0	0
DUTPE	26	0	0	ī	П	0	0	0	1	0		0
ORY C	27	0	0	0	0	0	0	0	0	0	0	0
MEM	28	-	-	1	0	0	0	-	0	1	0	-
ONLY	29	7	0	0	0	П	-	0		0	0	-
READ-ONLY MEMORY OUTPUT BITS	210	1	0	-	0	-	0	0	-	-	-	7
-	211	0	0	0	0	0	0	-	0	0	0	0
	212	1	0	0	-	1	0	0	-	0	-	~
	213	1	0	0	0	0	1	-	-	0	0	-
	214	0		1	-	1	1	-	-	0	0	0
	215	0	0	0	0	0	0	0	0	-	-	0
FREO	(HZ)	371.5	412.1	457.1	507.0	562.3	623.7	691.8	767.4	851.1	944.1	371.5
36	3⊢ 1			ER	N N		0	-	7	3	4	2
NUMBER "MODEN" 36	& ALERT CENTRAL			UPPER	ONES				LOWER	ONES		
UN QI	8 5	0	-	~	3	4	5		LOV	5		
KEYBOARD NUMBER	MODEN.	0	-	2	m	4	5	9	-	∞	6	0
TONE	NUMBER	0	-	7	m	4	5	9	2	∞	6	0
TONE	GROUPS	-		(OC)	>	-	*		(OC)			>
	9	4				— a	(00)					>

Table 18. Tone Group Z(QC), Z(QC)U, and Z(QC)L Frequencies and ROM Outputs

## ## ## ## ## ## ## ## ## ## ## ## ##	TOME	KEYBOARD NUMBER	UN QI	MBER DEN!" 26	1	FREO					R	READ-ONLY MEMORY OUTPUT BITS	NLY	MEMC	BY 0	UTPU	T BITS	10				
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	 UMBER	"MODEN"	282	ALERT NTRAL		(Hz)	215	214	213	212	211	210	29	28	27	26	25	24	23		21	20
1	0	0	0			346.7	0	0	1	-	0	П	0	0	0	-		0	0	-	_	-
2 10 10 10 10 10 10 10	-	p==1	-			384.6	0	0	-	7	-	0	0	0	0	-	0	0	0			0
3 3 TONES 473.2 0 1 0 0 1 1 1 1 0 0 0 1 1 0 0 0 1 0 0 0 1 0 0 0 1 0	2	2	2	UPPER	~	426.6	0	٦	0	0	0	0	1	0	0	-	-	0	0			0
4	3	m	3	TONES	S	473.2	0	-	0	0	0	1	Н	-	0	0	-	1	0	0	-	0
6 LOWER 2 716.1 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	4	4	4			524.8	0	1	0	1	0	0	1	0	0	-	0	0	7	0	0	0
6 LOWER POWER 2 716.1 0 1 1 0 0 1 0 0 1 0 1 1 0 1 1 0 1 1 0 0 1 1 0 0 1 1 0	5	2	22		0	582.1	0	1	0	-	1	0	0	0	0	0	-	0	0	0	0	-
7 LOWER 9 2 716.1 0 1 1 0 0 0 1 1 0 0 0 1 1 0 <th< td=""><td>9</td><td>9</td><td></td><td>]</td><td></td><td>645.7</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>-</td><td>0</td><td>0</td><td>0</td><td></td><td>0</td><td>7</td><td>0</td><td>7</td><td>-</td><td>-</td></th<>	9	9]		645.7	0	1	1	0	0	-	0	0	0		0	7	0	7	-	-
8 TONES 3 794.3 0 1 1 1 1 0 0 1 0 1 0 0 1 0 0 0 0 0 0	7	7	ro		2	716.1	0	1	1	1	0	0	0	1	0	-	-	0	0	0	0	p=4
9 4 881.0 1 0	8	œ	TO	NES <	3	794.3	0	1	1	1	1	0	0	1	0	-	0	0	0	0	-	
0 (5 346.7 0 0 1 1 0 0 0 0 0 1 1 0 0 0 1 1 1 0 0 1 1	6	6			4	881.0	-	0	0	0		0	0	0	0	0	0	-	0	0	0	0
	0	0			ر در	346.7	0	0		-	0	_	0	0	0	-	-	0	0	-	1	7

Table 19. Tone Group A(GE), A(GE)U, and A(GE)L Frequencies and ROM Outputs

	Į.											
	20		-	-	-	-	-	-				-
	21	0	0	0	0	0	0	0	0	0	0	0
	22	H	-	_	-	-	-	-	-	-	-	-
	23	0	0	0	0	0	0	0	0	0	0	0
S	24	0	0	-	0		0	-	-	-	-	0
T BIT	26	-	-	1	-1	-	-	-	-			-
UTPU	26	0	0	1	0	1	0	1	1	-	1	0
JRY C	27	0	0	0	0	0	0	0	0	0	0	0
MEM	28	0	1	1	0	0	-	_	0	0	-	0
JNLY	29	0	0	0	0	0	0	7	0	-	1	0
READ-ONLY MEMORY OUTPUT BITS	210	0	0	1	0	Н	0	0	1	0	0	0
R	211	-	1	0	0	0	-	0	0	0	0	7
	212	0	1	1	0	0	0	_	1	_	0	0
	213	1	0	1	0	0	0	0	0	_	-	-
	214	1	1	1	0	0	0	0	1	-	-	-
	215	0	0	0	1	1		1	0	0	0	0
FREO	(Hz)	682.5	592.5	757.5	802.5	847.5	892.5	937.5	547.5	727.5	637.5	682.5
20	8-4			E	ES		0		2	3	4	22
NUMBER "MODEN" 36	& ALERT CENTRAL			UPPER	TONES				/ER	TONES		
ID NOI	828	0	-	7	3	4	5		LOV	TO		
KEYBOARD NUMBER	"MODEN"	0	-	2	8	4	5	9	7	&	6	0
TONF	NUMBER	0	-	2	3	4	5	9	7	∞	6	0
	S						4		-∢	(GE)		>
TONE	GROUPS	~		A C)))		>					
	Ö	4				_	A (GE)					->
		11										

Table 20. Tone Group B(GE), B(GE)U, and B(GE)L Frequencies and ROM Outputs

			KEYBOA	KEYBOARD NUMBER	2						1											Γ
F	TONE	TONE	"MACORA"	"MODEN" 36	1'' 36	FREQ					Z.	AD-0	NLY	READ-ONLY MEMORY OUTPUT BITS	% O∩	TPUT	BITS					
GR	GROUPS	NUMBER	100 100	& ALERT CENTRAL	RT	(Hz)	215	214	213	212	211	210	29	28	27	26 2	25 2	24	23 2	22 2	21 2	20
4	4	0	0	0		652.5	0			0	0	-	0	-	0	0		0	0			
		~	-	-		607.5	0		-	0	0	0	0	0	0	-	-		0		0	
	GE)	2	7	2 \ 0.5	UPPER	787.5	0	-	-	-	-	0	0	0	0	1	1	-	0		0	-
	D -	ю	m	3 (ONES	832.5	1	0	0	0	0	0	-	1	0	0	1. (0	0		0	
α		4	4	4		877.5	-	0	0	0	0	-			0	1	-		0	1	0	
(GE)	*	5	5	5	0	922.5	1	0	0	-	0	0	1	0	0	0	1	0	0	-	0	-
		9	9		-	967.5	0	М	0		0			0	0			-	0	-	0	
	B (2	7	7	LOWER	7	517.5	0	7	0		0	0	0	1	0	1	-		0	-	0	
	(GE)	∞	œ	TONES	3	562.5	0	-	0	-	0	1	1	0	0	0		0	0	H	0	
		6	6		4,	697.5	0	-	П	0		0	0	1	0]	-	0 1		0	
>	->	0	0		22	652.5	0			0	0	7	0	1	0	0	1 0		0		0	

Table 21. Tone Group C(GE), C(GE)U, and C(GE)L Frequencies and ROM Outputs

	7	Ti .	1			T		1	1		i	
	20	-	-	-		_		-	-		-	
	21	0	0	0	0	0	0	0	0	0	0	0
	22	-		~			-	-	-		-	-
	23	0	0	0	0	0	0	0	0	0	0	0
S	24	-	0	0	1	0		0	0	1	0	-
JT BIT	25	1	1	1	1	-	1	1	-	1	-	7
OUTP	26	1	0	0	1	0	-	0	0	7	0	-
ORY (27	0	0	0	0	0	0	0	0	0	0	0
MEM	28	0	П	7	П	0	0		-	1	0	0
ONLY	29	-	0	1	0	1	0	0	-	-	1	
READ-ONLY MEMORY OUTPUT BITS	210		0	1	0	1	0	1	0	-	0	-
	211	0	0	0	0	0	0	0	0	0	0	0
	212	0	П,	1	0	0	1	П	1		0	0
	213	1	П	1	0	0	0	0	0	0	1	7
	214	1	1	-	0	0	0	0	П	1	П	7
	215	0	0	0	1	1	1	1	0	0	0	0
FREQ	(Hz)	667.5	712.5	772.5	817.5	862.5	907.5	952.5	532.5	577.5	622.5	667.5
KEYBOARD NUMBER	& ALERT CENTRAL	0	-	2 VPPER	3 (IONES	4	5) (0	parad.	LOWER 2	TONES 3	4	5
KEYBOA	100	0	prod	2	8	4	5	9	2	œ	6	0
TONE	NUMBER	0	-	2	8	4	5	9	2	_∞	6	0
TONE	GROUPS	4		(GE)	>-		(GE)		် (၁)	7		>

INSTALLATION

UNPACKING AND INSPECTION

As soon as possible after delivery, unpack the equipment and inspect it thoroughly. If any part of the equipment has been damaged in transit, report the extent of the damage to the transportation company immediately.

This unit has been inspected and adjusted to its recommended operating condition at the factory. Unless it has been handled roughly in transit or otherwise abused or tampered with, it will require only line output adjustments, which are dependent upon the system audio line requirements. This adjustment is described in the "Preoperational Adjustments" paragraph of this section.

2. PRELIMINARY EQUIPMENT CHECKS

- a. Check the mechanical operation of all keyboard pushbuttons to ensure that they operate without binding.
- b. Remove the top cover on the paging encoder housing by removing four #6 screws which are accessible from the underside of the unit (see Figure 2).

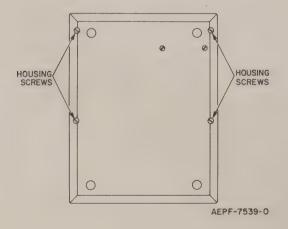


Figure 2. Housing Screw Locations

NOTE

The paging encoder housing (top and bottom) is interconnected by a cable.

- c. Carefully remove the top cover of the housing and place it beside the bottom portion of the housing.
- d. The display board is plugged into the main circuit board; ensure that it is firmly in place.
- e. Ensure that there are no loose nor broken wires.
- f. Temporarily reassemble the paging encoder housing so that the unit can be checked according to the instructions in the "Preoperational Check" paragraph later in this section.

3. GENERAL INSTALLATION REQUIREMENTS

To ensure optimum performance and reliability, adequate facilities must be available at the paging encoder location. Carefully review the electrical and physical requirements outlined in the following paragraphs before selecting a site for the paging encoder installation.

a. Physical Requirements

Ambient temperature in the paging encoder room must be maintained between 32 and 120 degrees Fahrenheit (0 and 49 degrees Celcius). Relative humidity should remain between 45 and 95 percent. Under no circumstances should condensation be allowed.

The paging encoder should not be subjected to vibration nor shock. Do not install the paging encoder in rooms adjoining machine shops, printing presses, refrigeration equipment, nor other similar types of high electrical noise or vibration. In some locations, filtering may be required to maintain a low dust area.

b. Electrical Requirements

(1) Power Connections

(a) AC Power Source

The paging encoder is factory wired for 117 volts ac, 60 Hertz operation or 234 volts ac, 50 Hertz operation. If a 234-volt ac power source is to be used, the 117-volt ac plug must be cut from the ac line cord and the appropriate 234-volt ac plug attached.

A three-wire power system or appropriate grounded plug adapter must be used.

(b) DC Power Source

If a dc power source is to be used, the paging encoder requires a 12- to 18-volt do power source with a continuous current drain of 40 milliamperes minimum and 250 milliamperes maximum. The minimum current drain is measured by entering a paging call code into the keyboard: 11 for "Moden" 100 and 36 paging encoders. For Alert Central paging encoder, a one is entered, but the measurement is taken after the automatic page mode terminates. The maximum current drain is measured by entering a different paging call code into the keyboard (88 for "Moden" 100, 00 for "Moden" 36, and 0 (red pushbutton) for Alert Central); and then the keyboard page pushbutton is depressed. The maximum current drain measurement is taken during the paging mode.

The paging encoder does not include fuse protection for the dc input power source; therefore, cable TKN6323 is recommended because it has a built-in fuse. Connection of the dc power source must be made to main circuit board screw terminals DC+ and GND.

NOTE

Observe polarity when connecting a power source to the paging encoder. If the polarity is reversed, the logic circuitry will be inoperative.

(2) Interference

As with any complex electronic facility, the performance of this paging encoder may be degraded by spurious signals received from outside sources. Minimize the possibility of interference by selecting a paging encoder location away from generators of electrical noise such as large motors, switchgear, welding equipment, etc.

The digital logic circuitry used in the paging encoder, although immune to most low-level interference, is particularly susceptible to discharges of static electricity. These discharges, which often reach high potentials, introduce errors and may cause erratic operation. Nonconductive household carpeting provides an excellent medium for the generation of static potentials and this type of floor covering is NOT recommended for use at the paging encoder site. It is recommended that conductive carpeting or tile, manufactured especially for electronic installations, be used in the paging encoder site. If a conductive floor

covering is not used, the area around the paging encoder must be sprayed with an antistatic compound at least once a week during periods of low humidity. A suitable chemical is supplied in spray cans under the brand name "Static-Stop," manufactured by Barco Chemical Products, Chicago, Illinois. Other equivalent products are available and these should serve just as well. However, be sure that the product will not damage the floor covering nor the paging encoder housing.

4. PREOPERATIONAL CHECK

a. "Moden" 100 and "Moden" 36 Paging Encoder

- (1) Plug the paging encoder into an ac power source and set the AC-OFF-DC switch to the AC position. The digit display should be "00."
- (2) Enter a two-digit number into the paging encoder using the numbered keyboard pushbuttons. Note that the numbers are displayed from right to left as they are entered.
- (3) Depress the keyboard page (P) pushbutton and note that the PAGE indicator lamp begins to glow.
- (4) The PAGE indicator lamp stops glowing after the paging mode is automatically terminated. On the "Moden" 100 paging encoder, note that the TALK indicator lamp begins to glow. The TALK lamp continues to glow until the unit is switched off. (When either JUl or 2 is cut, the TALK light will illuminate during the talk cycle for eight to ten seconds.
- (5) Set the AC-OFF-DC switch to the OFF position and unplug the paging encoder from the power source.

b. Alert Central Paging Encoder

- (1) Plug the paging encoder into an ac power source and set the AC-OFF-DC switch to the AC position. The digit display should be "0."
- (2) Depress a numbered keyboard pushbutton. Note that the number depressed is displayed and the PAGE indicator lamp begins to glow. Approximately four to six seconds later the PAGE lamp stops glowing.
- (3) Set the AC-OFF-DC switch to the OFF position and unplug the paging encoder from the power source.

5. MOUNTING

The paging encoder can be placed on any flat, level, surface such as a desk top which provides the operator full visibility of all keyboard pushbuttons and indicators.

6. OPTIONAL JUMPER AND TONE TIMING RESISTOR CONFIGURATIONS

Optional jumper and tone timing resistor configurations on the main circuit board are described here. Not all jumpers are covered in this description; the schematic diagram shows jumper differences between models of the paging encoders described in this manual.

Remove the top cover of the paging encoder housing as described in "Preliminary Equipment Checks" of this section. Refer to Figure 3 for jumper locations.

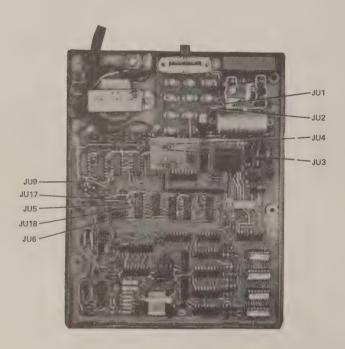


Figure 3. Optional Jumper Locations

a. Optional Jumpers

(1) Jumper JUl

Jumper JUl is used for carrier squelch systems and cut out for PL squelch systems.

(2) Jumper JU2

Jumper JU2 is used for PL "Mocom," PL "Maxar," and PL "Compa-Station" base stations and cut out for all other Motorola base stations.

(3) Jumper JU3

Jumper JU3 is used for all except PL "'Mocom" and PL "Maxar" base stations where it is cut out.

(4) Jumper JU4

Jumper JU4 is used for PL "Maxar" base stations and cut out for all other base stations.

(5) Jumpers JU5 and JU6

Jumpers JU5 and JU6 are used for all "Moden" 100, "Moden" 36, and Alert Central paging encoders with fixed tone B and are cut out for Alert Central paging encoders with the fixed tone A option. These two jumpers are used in conjunction with jumpers JU17 and JU18.

(6) Jumper JU9

Jumper JU9 is used for all Alert Central paging encoders and cut out for all other "Moden" Paging Encoders described in the manual. When jumper JU9 is in, pin 8 of keyboard plug Pl (black wire) is tied back and not connected to plug Pl.

(7) Jumpers JU17 and JU18

Jumpers JU17 and JU18 are used for Alert Central paging encoders with the fixed tone A option and are cut out of all other "Moden" Paging Encoders described in this manual. These two jumpers are used in conjunction with jumpers JU5 and JU6.

b. Tone Timing Resistors

Depending upon the order, the paging encoder is shipped from the factory with the tone timing set for tone-only or tone-and-voice operation.

Table 22 lists resistors and values that are changed according to the timing desired.

The times shown in Table 22 are the times required by the paging receiver. In tone remote control systems, the RC time constant should account for the 200 milliseconds that tone A is muted while the transmitter turn-on tones are being sent.

Table 22. Tone Timing Resistor Values

		RESISTOR T	HAT TIMING IS	DEPENDENT ON	
SIGNALING		TONE A		TON	E B
MODE	TONE LENGTH	RESI:	STOR LUE	TONE LENGTH	RESISTOR VALUE
	(MINIMUM)	R19	R20	(MINIMUM)	R27
Tone-and-Voice	1.0 sec.	120 k	390 k	3.0 sec.	220 k
Tone-Only	.4 sec.	47 k	560 k	.8 sec.	68 k
Tone-Only with Battery Saver	2.7 sec.	390 k	560 k	.8 sec.	68 k
Subaudible	1.0 sec.	120 k	390 k	3.0 sec.	220 k

NOTE: Formulas for calculating tone timing are as follows.

• "Moden" 100, "Moden" 36, and Alert Central paging encoders

Tone A Timing = 1.1
$$(\frac{R19 \cdot R20}{R19 + R20})$$
 C7

Tone B Timing = 1.1(R27)C10

Group Call Timing = 1.1[R20(C7) + R27(C10)] (8s minimum)

• ''Moden'' 100 Paging Encoder

Gap Timing = 1.1(R29)C14

Talk Timing = 1.1(R31)C16

7. EXTERNAL CONNECTIONS

All external connections are made to screw-type terminals which are accessible when the top of the paging encoder housing is removed. A total of nine of these terminals are provided to handle all possible input and output connections associated with the encoder. Cable clamps are provided to secure the external connections to the paging encoder housing. The larger of the two cable clamps is used to hold both the microphone cable and the base station cable. If only the base station cable connects to the paging encoder, use the smaller cable clamp. All external connections should pass through the cable clamp at the point where all the wires enter the paging encoder housing (refer to Figure 4).

a. Microphone Connections

For tone and voice systems, either the TMN1004 Desk Microphone (carrier squelch systems) or the TMN1005 Desk Microphone (PL squelch systems) is required. Depending upon system operation, the appropriate microphone

cable wires must be connected as listed in Table 23. Unused wires must be tied back or cut. The "S" hook strain relief on the microphone cable is not used for this application; therefore, wrap tape around the cable and the strain relief hook so that it will not hook onto nor interfere with other cables.

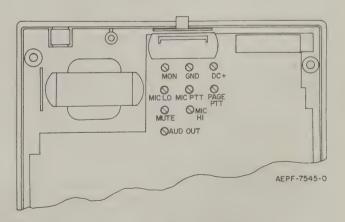


Figure 4.
External Connection Terminals

Table 23.
TMN1004 or TMN1005 Microphone Connections

WIRE COLOR	SIGNAL FUNCTION	PAGING ENCODER SCREW TERMINALS
Brown	Microphone Monitor	MIC HI
Shield	Microphone Low	MIC LO
Green	Push-To-Talk	MIC PTT
White	Microphone Monitor (On TMN1005 only)	MON
Black	Ground	GND
Yellow	8-Ohm Hot	Not Used
Red	8-Ohm Mute	Not Used

b. "Moden" Input-Output Screw Terminal Connections

The following paragraphs describe the function of the nine input and output screw terminal connections in the paging encoder.

- (1) MON This is used as a tie point for the microphone monitor lead and the base station PL disable lead. It does NOT connect internally to the paging encoder.
- (2) GND This is the circuit and chassis ground point.
- (3) DC+ This is used when operating the paging encoder from a 12- to 18-volt dc power source. The positive side of the dc power source connects to this point.
- (4) MIC LO This is used for a microphone ground connection or another circuit and chassis ground point.
- (5) MIC PTT The microphone push-to-talk lead connects to this point. In carrier squelch systems, jumper JUl is used, and the microphone transmit switch, when depressed, provides a closure to ground to energize paging encoder keying relay K2. When energized, keying relay K2 provides a ground closure to the base station push-to-talk lead. In "Private-Line" squelch systems, jumper JUl is removed, and the MIC PTT screw terminal becomes a tie point for the microphone and PL base station push-to-talk lines.
- (6) PAGE PTT This screw terminal provides a dry relay contact closure to ground when paging encoder keying relay K2 is energized. In carrier squelch base stations, this point ties to the base station push-to-talk terminal. In PL

base stations, it ties to the terminal which when grounded disables the base station from transmitting with PL tone. This contact closure is rated at 10 volt-amperes.

- (7) MUTE This screw terminal provides a dry relay contact closure to ground when paging encoder paging relay K1 is energized. Paging relay K1 is energized only during the paging tone generation mode. In installation this point ties to the MIC HI terminal of a remote control console. This contact closure is rated at 10 volt-amperes.
- (8) MIC HI The microphone-high lead of the microphone ties to this screw terminal. This point ties internally to a normally closed relay contact of paging encoder paging relay K1. Paging relay K1 in its de-energized state connects the MIC HI screw terminal directly to screw terminal AUD OUT. The base station audio input terminal is connected to the paging encoder AUD OUT screw terminal to provide dc bias current for the microphone and, therefore, care must be taken to observe polarities when connecting cables.
- (9) AUD OUT The audio output screw terminal of the paging encoder is a tie point for the base station audio input terminal. This point ties internally to a wiper contact of paging relay K1. When K1 is de-energized, this point ties directly to the paging encoder MIC HI screw terminal. When K1 is energized, this point is capacitively coupled to the low impedance paging tone output amplifier.

c. Base Station Connections

(1) Local Control

To connect the paging encoder to a local control base station or remote control console for remote base station systems, use the TKN6065 Cable Kit. Figures 5 through 13 illustrate typical connections for the most common types of equipment. If your installation differs, refer to the instruction manual for your particular system.

(2) Subaudible Connections

Figures 14 and 15 illustrate typical interconnections between the paging encoder and the base station when subaudible paging operation is to be used. Figure 14 shows the connections required in a local control console setup using the NLN8240 Subaudible Interface Kit; Figure 15 shows connections for a remote control console setup using the SP57011801 Subaudible Remote Kit.

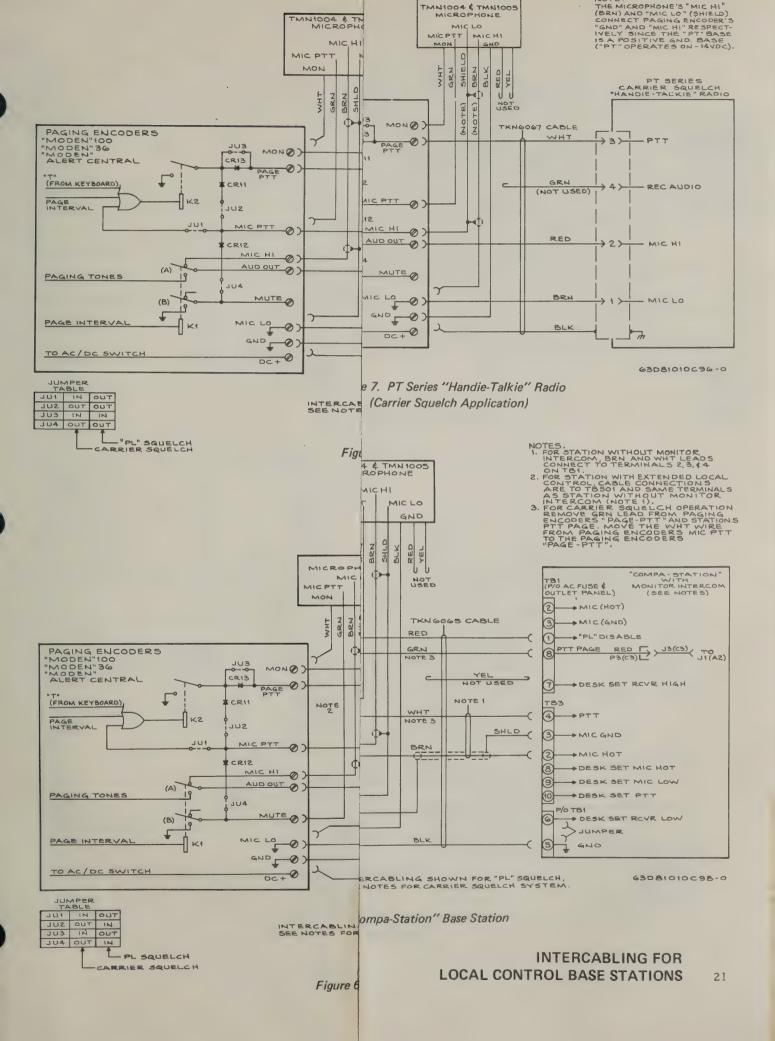


Table 23.
TMN1004 or TMN1005 Microphone Connections

WIRE COLOR	SIGNAL FUNCTION	PAGING ENCODER SCREW TERMINALS
Brown	Microphone Monitor	MIC HI
Shield	Microphone Low	MIC LO
Green	Push-To-Talk	MIC PTT
White	Microphone Monitor	MON
	(On TMN1005 only)	
Black	Ground	GND
Yellow	8-Ohm Hot	Not Used
Red	8-Ohm Mute	Not Used

b. "Moden" Input-Output Screw Terminal Connections

The following paragraphs describe the function of the nine input and output screw terminal connections in the paging encoder.

- (1) MON This is used as a tie point for the microphone monitor lead and the base station PL disable lead. It does NOT connect internally to the paging encoder.
- (2) GND This is the circuit and chassis ground point.
- (3) DC+ This is used when operating the paging encoder from a 12- to 18-volt dc power source. The positive side of the dc power source connects to this point.
- (4) MIC LO This is used for a microphone ground connection or another circuit and chassis ground point.
- (5) MIC PTT The microphone push-to-talk lead connects to this point. In carrier squelch systems, jumper JUl is used, and the microphone transmit switch, when depressed, provides a closure to ground to energize paging encoder keying relay K2. When energized, keying relay K2 provides a ground closure to the base station push-to-talk lead. In "Private-Line" squelch systems, jumper JUl is removed, and the MIC PTT screw terminal becomes a tie point for the microphone and PL base station push-to-talk lines.
- (6) PAGE PTT This screw terminal provides a dry relay contact closure to ground when paging encoder keying relay K2 is energized. In carrier squelch base stations, this point ties to the base station push-to-talk terminal. In PL

base stations, it ties to the terminal which when grounded disables the base station from transmitting with PL tone. This contact closure is rated at 10 volt-amperes.

- (7) MUTE This screw terminal provides a dry relay contact closure to ground when paging encoder paging relay Kl is energized. Paging relay Kl is energized only during the paging tone generation mode. In installation this point ties to the MIC HI terminal of a remote control console. This contact closure is rated at 10 volt-amperes.
- (8) MIC HI The microphone-high lead of the microphone ties to this screw terminal. This point ties internally to a normally closed relay contact of paging encoder paging relay Kl. Paging relay Kl in its de-energized state connects the MIC HI screw terminal directly to screw terminal AUD OUT. The base station audio input terminal is connected to the paging encoder AUD OUT screw terminal to provide dc bias current for the microphone and, therefore, care must be taken to observe polarities when connecting cables.
- (9) AUD OUT The audio output screw terminal of the paging encoder is a tie point for the base station audio input terminal. This point ties internally to a wiper contact of paging relay K1. When K1 is de-energized, this point ties directly to the paging encoder MIC HI screw terminal. When K1 is energized, this point is capacitively coupled to the low impedance paging tone output amplifier.

c. Base Station Connections

(1) Local Control

To connect the paging encoder to a local control base station or remote control console for remote base station systems, use the TKN6065 Cable Kit. Figures 5 through 13 illustrate typical connections for the most common types of equipment. If your installation differs, refer to the instruction manual for your particular system.

(2) Subaudible Connections

Figures 14 and 15 illustrate typical interconnections between the paging encoder and the base station when subaudible paging operation is to be used. Figure 14 shows the connections required in a local control console setup using the NLN8240 Subaudible Interface Kit; Figure 15 shows connections for a remote control console setup using the SP57011801 Subaudible Remote Kit.

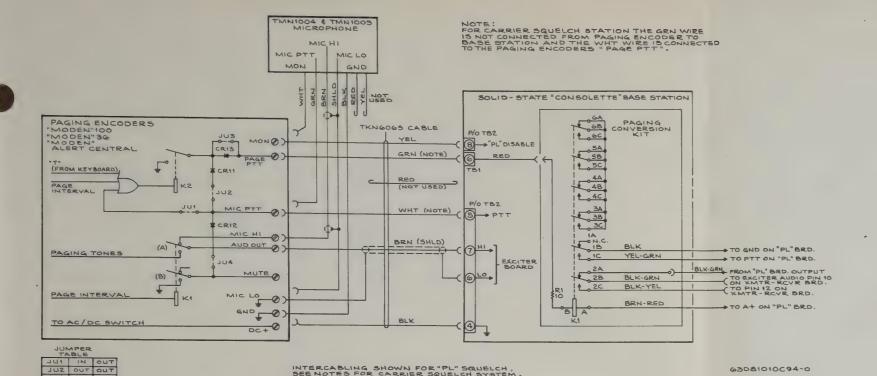


Figure 5. "Consolette" Base Station

NOTES:

1. FOR CARRIER SQUELCH THE RED WIRE IS NOT CONNECTED TO ENCODER AND THE GRN WIRE CONNECTS TO ENCODER'S "PAGE PTT."

2. FOR CARRIER SQUELCH THE MICROPHONE'S GRN WIRE CONNECTS TO THE PAGING ENCODER'S "MIC PTT" TERMINAL.

3. CONNECTS CEN PROVIDES CURRENT ISOLATION DETWEEN TO THE MAXAR.

4. CR12 IS PROVIDED TO MAINTAIN A DIODE DROP TO GND POTENTIAL AT THE MAXAR "PTT" INPUT WHEN KEYING THROUGH THE MICROPHONE. MICPTT MIC LC MON GNO

PL" SQUELCH

L PL SQUELCH CARRIER SQUELCH

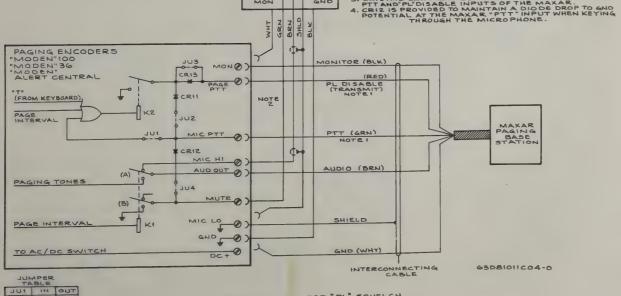


Figure 6. "Maxar" Base Station

INTERCABLING FOR "PL" SQUELCH, SEE NOTES FOR CARRIER SQUELCH CONNECTIONS.

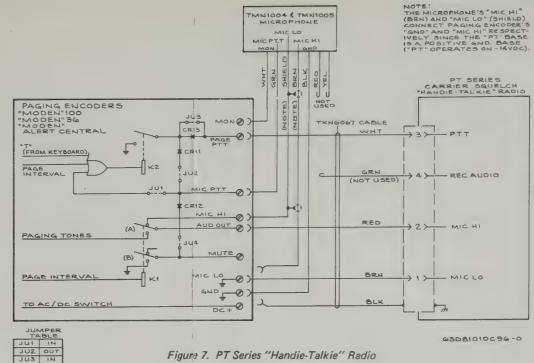
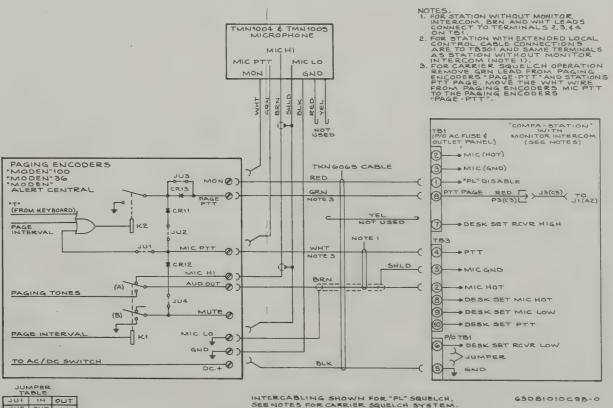


Figure 7. PT Series "Handie-Talkie" Radio (Carrier Squelch Application)

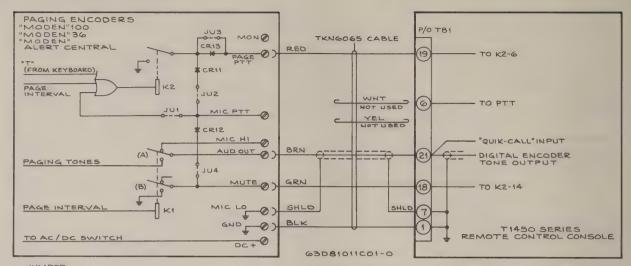


JUI IN OUT JUZ OUT IN JU3 IN IN L PL SQUELCH -CARRIER SQUELCH

Figure 8. "Compa-Station" Base Station

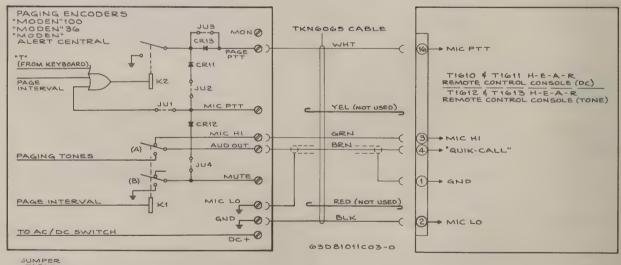
INTERCABLING FOR LOCAL CONTROL BASE STATIONS T1360
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+ TO T8-17)
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ED WHEN
IT 13

PAGING AND ADD MTB-17 OLE.



JUMPER TABLE JUI IN JUZ OUT JU3 IN

Figure 11. T1450 Series Remote Control Console ("HEAR")



JUMPER TABLE

JUI IN OUT

JU2 OUT OUT

JU3 IN IN

JU4 OUT OUT

PL SQUELCH

CARRIER SQUELCH

Figure 12. T1600 Series Remote Control Console ("HEAR")

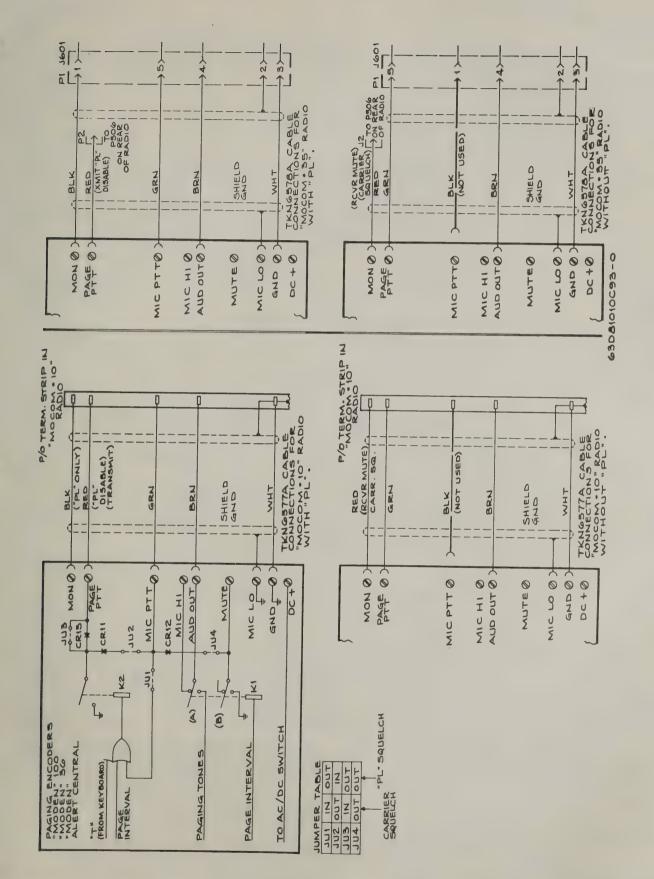


Figure 13. "Mocome10" and "Mocome35" FM Radio

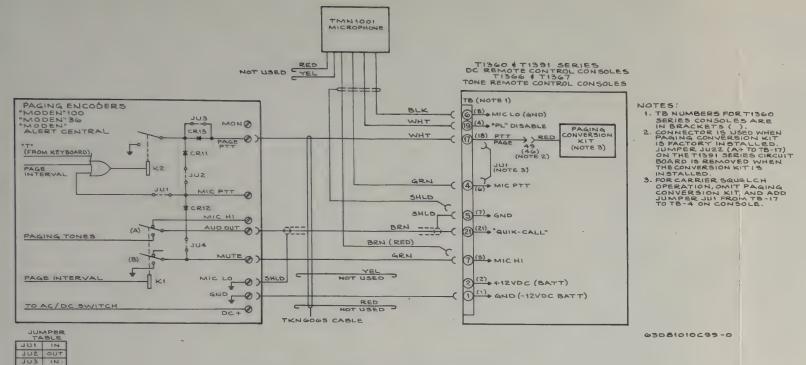


Figure 9. T1300 Series Remote Control Console (DC and Tone)

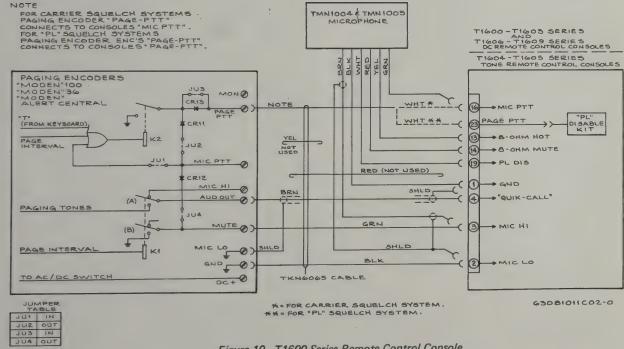
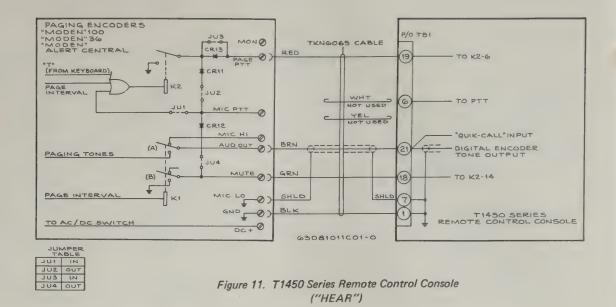
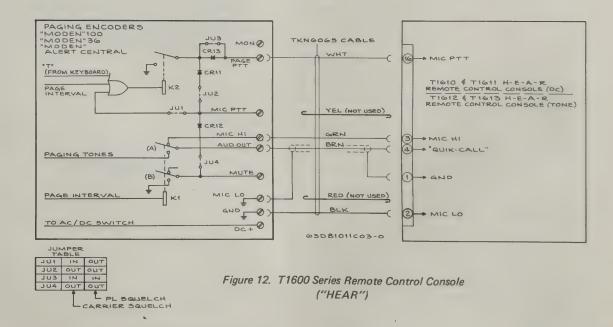


Figure 10. T1600 Series Remote Control Console (DC and Tone)





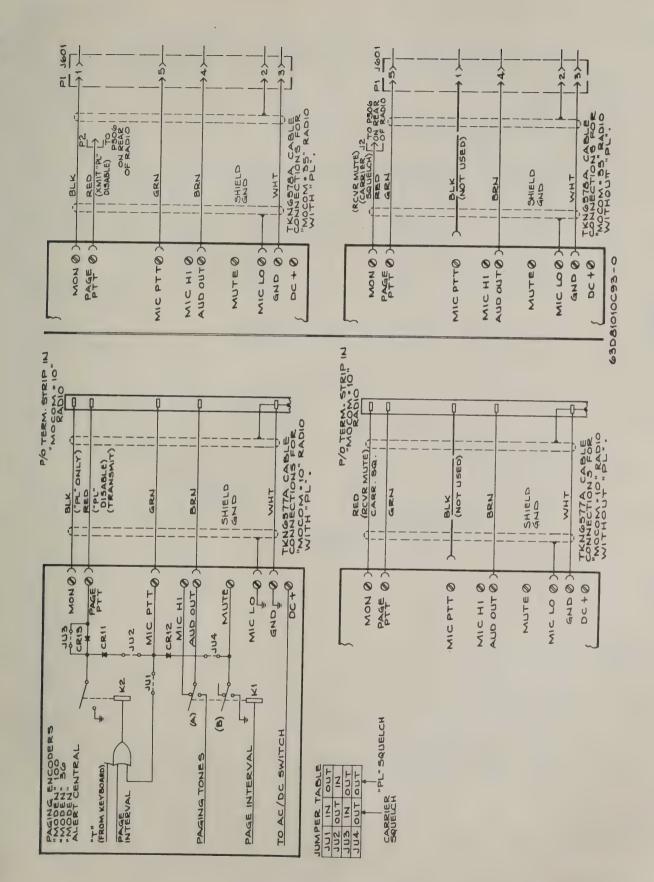


Figure 13. "Mocome10" and "Mocome35" FM Radio

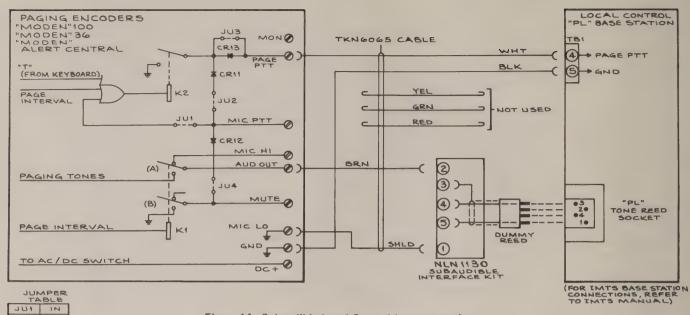


Figure 14. Subaudible Local Control Interconnections

63D81010C97-0

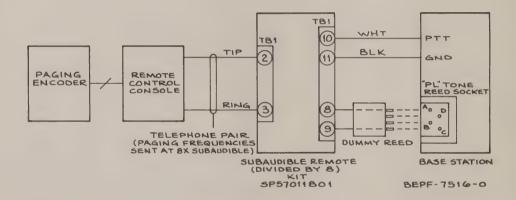


Figure 15. Subaudible Remote Control Interconnections

(3) Multiple Paging Encoder Connections

Multiple paging encoders can be connected together as shown in Figure 16. Only two cables can fit in a paging encoder; therefore, in parallel operation, one paging encoder should be connected to the microphone and the other to the base station. Use the TKN6065 Cable Kit to connect one paging encoder to another.

8. PREOPERATIONAL ADJUSTMENTS

NOTE

Recommended test equipment is listed in the "Maintenance" section of this manual.

Variable resistor R84 on the main circuit board adjusts the paging tone audio level to the base station. Refer to paragraph 8. a. to adjust the output level. Paragraph 8. b. describes the output level adjustment for the Alert Central paging encoder with fixed tone B (standard models).

a. "Moden" 100, "Moden" 36, and Alert Central (Fixed Tone A) Paging Encoders

NOTE

Alert Central (Fixed Tone A) is available as factory option R176AA.

(1) Remove the top cover on the paging encoder housing by removing four #6 screws which are accessible from the underside of the unit (see Figure 2).

JUZ OUT
JU3 IN
JU4 OUT

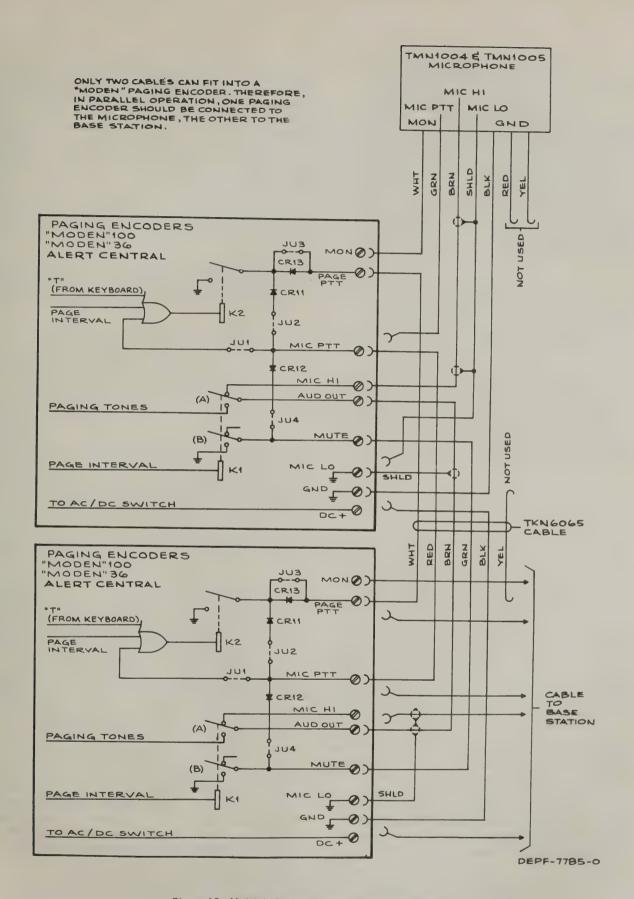


Figure 16. Multiple Paging Encoder Interconnections

- (2) Carefully remove the top cover of the housing and place it beside the bottom portion.
- (3) From the label on the bottom of the paging encoder, determine the tone group or specific frequencies that have been coded into the paging encoder. If a tone group is specified, refer to the "Tone Coding" section for the specific tone group table listing the specific frequencies for that particular tone group. If a particular tone group was not used, then the label on the bottom of the paging encoder should list the specific frequencies for its associated keyboard pushbutton.
- (4) From the tone group frequencies, choose the highest, lowest, and middle range frequencies; note the corresponding keyboard pushbuttons. For example, for tone group one in a "Moden" 100 paging encoder, the highest frequency is 539.0 Hz and the lowest frequency is 330.5 Hz; these frequencies will be different in a "Moden" 36 and Alert Central paging encoder. The middle range of the highest and lowest frequencies is derived by subtracting the lowest frequency from the highest frequency, dividing by two, and adding the answer to the lowest frequency or subtracting it from the highest frequency:

$$MF = \frac{HF - LF}{2} + LF$$
 or $MF = HF - \frac{HF - LF}{2}$.

After deriving the middle frequency of the tone group, determine which tone frequency is closest to the calculated middle frequency. Using the preceding "Moden" 100 paging encoder example, the middle frequency of tone group one should have been calculated to be 434.75 Hz. Checking the tone group one table, 433.7 Hz is the closest frequency to the calculated middle frequency. Therefore, for tone group one, keyboard 0 produces the lowest frequency, 5 produces the middle frequency, and 9 produces the highest frequency. For tone group three, after selecting the lowest frequency and highest frequency and calculating the middle frequency, we find that keyboard l produces the lowest frequency, keyboard 5 produces the middle frequency, and keyboard 0 produces the highest frequency. The lowest, middle, and highest frequencies of each tone group can be determined in the preceding manner.

- (5) Refer to the circuit board detail; locate test point TPl and jumper it to ground. By grounding test point TPl, tone B, the right-hand digit of the display, will be generated for as long as test point TPl is grounded.
- (6) Enter the middle frequency of the paging encoder tone group by depressing its corresponding keyboard pushbutton.
- (7) Using a service monitor (monitors base station transmission), adjust R84 for a frequency deviation of ±3.3 kHz.
- (8) Enter the high and low frequencies of the paging encoder and record their readings in the same manner as done for the middle frequency.

NOTE

A deviation of ±3.3 kHz is a typical setting (±0.75 kHz for subaudible). It is recommended that the appropriate pager manual be consulted for proper deviation settings. For further information, refer to Service and Repair Notes Bulletin SRN-514, August 1974.

- (9) Adjust the deviation (R84) such that the worst reading is ±3.3 kHz. Also ensure that the highest reading is not displaying a clipped waveform on the service monitor. If ±3.3 kHz cannot be attained or a clipped waveform is shown when setting for a minimum of ±3.3 kHz, adjust R84 for a minimum setting of ±2 kHz. If ±2 kHz cannot be attained, continue to the following paragraph.
- (10) If a minimum deviation of ±2 kHz cannot be attained and the frequencies are correct, it could be that the paging encoder is not providing sufficient signal to the base station. Typically, the base station requires . 165 volt rms for 60% or ±3.0 kHz deviation. The "Moden" paging encoders provide a de-emphasized (6 dB/octave) paging tone to the base station. If the generated frequencies are 2 kHz or greater, then capacitor C30 (.068 uF) may have to be removed. The paging tones will then be fed to the base station "flat." The de-emphasis characteristic of capacitor C30 is necessary to offset the base station pre-emphasis characteristic, but if in the group of frequencies to be generated there exists less than an octave difference, de-emphasis is not necessary. If the encoder is supplying sufficient signal to the base station, consult the signal and adjustment section of the base station instruction manual.

- (11) On tone and voice models, key the base station with the microphone. Speak normally into the microphone at a distance of about eight inches. Check the service monitor for a deviation of ±3.3 kHz. See the microphone instruction manual for level adjustments if ±3.3 kHz cannot be attained.
- (12) Remove the ground jumper from TPl and reassemble the paging encoder.

b. Alert Central Paging Encoder (Fixed Tone B)

- (1) Remove the top cover on the paging encoder housing by removing four #6 screws which are accessible from the underside of the unit (see Figure 2).
- (2) Carefully remove the top cover of the housing and place it beside the bottom portion.
- (3) From the label on the bottom of the paging encoder, determine the tone group or specific frequencies that have been coded into the paging encoder. If a tone group is specified, refer to the "Tone Coding" section for the specific tone group table listing the specific frequencies for that particular tone group. If a particular tone group was not used, then the label on the bottom of the paging encoder should list the specific frequencies for its associated keyboard pushbutton.
- (4) From the tone group frequencies, choose the highest, lowest, and middle range frequencies; note the corresponding keyboard pushbuttons. For example, for tone group one in a "Moden" 100 paging encoder, the highest frequency is 539.0 Hz and the lowest frequency is 330.5 Hz; these frequencies will be different in a "Moden" 36 and Alert Central paging encoder. The middle range of the highest and lowest frequencies is derived by subtracting the lowest frequency from the highest frequency, dividing by two, and adding the answer to the lowest frequency or subtracting it from the highest frequency:

Let LF = Lowest Frequency
MF = Middle Frequency
HF = Highest Frequency

$$MF = \frac{HF - LF}{2} + LF$$
 or $MF = HF - \frac{HF - LF}{2}$.

After deriving the middle frequency of the tone group, determine which tone frequency is closest to the calculated middle frequency. Using the preceding "Moden" 100 paging encoder example, the middle frequency of tone group one should have been

calculated to be 434.75 Hz. Checking the tone group one table, 433.7 Hz is the closest frequency to the calculated middle frequency. Therefore, for tone group one, keyboard 0 produces the lowest frequency, 5 produces the middle frequency, and 9 produces the highest frequency. For tone group three, after selecting the lowest frequency and highest frequency and calculating the middle frequency, we find that keyboard 1 produces the lowest frequency, keyboard 5 produces the middle frequency, and keyboard 0 produces the highest frequency. The lowest, middle, and highest frequencies of each tone group can be determined in the preceding manner.

- (5) Refer to the circuit board detail; locate the positive (+) side of capacitor C7 and jumper it to ground. Tone A will be generated for as long as the positive side of capacitor C7 is grounded.
- (6) Enter the middle frequency of the paging encoder tone group by depressing its corresponding keyboard pushbutton.
- (7) Using a service monitor (base station transmission), adjust R84 for a frequency deviation of ±3.3 kHz.
- (8) Momentarily turn power off for a few seconds. This must be done every time the paging code is to be changed during this adjustment.
- (9) Enter the high and low frequencies of the paging encoder and record their readings in the same manner as the middle frequency.

NOTE

A deviation of ±3.3 kHz is a typical setting (±0.75 kHz for subaudible). It is recommended that the appropriate pager manual be consulted for proper deviation settings. For further information, refer to Service and Repair Notes Bulletin SRN-514, August 1974.

- (10) Adjust the deviation (R84) such that the worst reading is ±3.3 kHz. Also ensure that the highest reading is not displaying a clipped waveform on the service monitor. If ±3.3 kHz cannot be attained or a clipped waveform is shown when setting for a minimum of ±3.3 kHz, adjust R84 for a minimum setting of ±2 kHz. If ±2 kHz cannot be attained, continue to the following paragraph.
- (11) If a minimum deviation of ±2 kHz cannot be attained and the frequencies are correct, it could be that the paging encoder is not providing

sufficient signal to the base station. Typically, the base station requires . 165 volt rms for 60% or ±3.0 kHz deviation. The "Moden" paging encoders provides a de-emphasized (6 dB/octave) paging tone to the base station. If the generated frequencies are 2 kHz or greater, then capacitor C30 (.068 uF) may have to be removed. The paging tones will then be fed to the base station "flat." The de-emphasis characteristic of capacitor C30 is necessary to offset the base station pre-emphasis characteristic, but if in the group of frequencies to be generated there exists less than an octave difference, de-emphasis is not necessary. If the encoder is supplying sufficient signal to the base station, consult the signal and adjustment section of the base station instruction manual.

(12) On tone and voice models, key the base station with the microphone. Speak normally into the microphone at a distance of about eight inches. Check the service monitor for a deviation

of ±3.3 kHz. See the microphone instruction manual for level adjustments if ±3.3 kHz cannot be attained.

(13) Remove the ground jumper from the positive side of capacitor C7 and reassemble the paging encoder.

9. READ-ONLY MEMORY FIELD OPTION INSTALLATION

The NLN1442A and NLN1435A Read-Only Memory Kits consist of four or two ROMs and a coding label. To install a kit, remove the top cover on the paging encoder housing by removing four #6 screws (refer to Figure 2). Remove the presently-installed plug-in ROMs on the main circuit board (see "Circuit Board Detail" for ROM location). Plug the new ROMs into the proper sockets being careful to orient pin 1 of the IC package with the "dot" on the circuit board. Place the top cover back in position and secure with the four screws. Affix the coding label to the underneath surface of the paging encoder.

OPERATION

1. INTRODUCTION

This section of the manual covers controls and indicators and operation of the three paging encoder models: "Moden" 100, "Moden" 36, and Alert Central.

2. CONTROLS AND INDICATORS

The controls and indicators for the three "Moden" paging encoder models are physically different as shown in Figure 17. The specific functions of the controls and indicators are identical except where specifically noted.

a. Keyboard

(1) Numbered Keyboard Pushbuttons - momentary pushbutton switches used to enter the paging receiver cap code (individual or group call code number). On "Moden" 100 and "Moden" 36 Paging Encoders, a group call is generated when the entered digits are the same (22, 66, 00, etc.). The red keyboard pushbutton of the Alert Central paging encoder acts as the group call function; it displays a zero on the paging encoder display when pushed.

(2) P (page) - a momentary pushbutton switch used to initiate the paging cycle. For the Alert Central, the paging cycle is automatic; therefore, the P (page) pushbutton is inoperable.

NOTE

The Alert Central automatic paging function can be disabled so that paging can be initiated by depressing the page pushbutton. Refer to "Setup Procedures" in the "Installation" section.

(3) T (talk) - a momentary pushbutton switch which is momentarily depressed to shorten the automatic talk cycle or is held down to extend the talk cycle duration of a voice message when using a "Moden" 100 paging encoder. For the "Moden" 36 and Alert Central paging encoders, the talk (T) pushbutton must be depressed before the page lamp goes out and held down for the duration of the voice message.

b. Indicators

(1) Digit Display - displays the pager code number entered with the keyboard pushbutton switches.

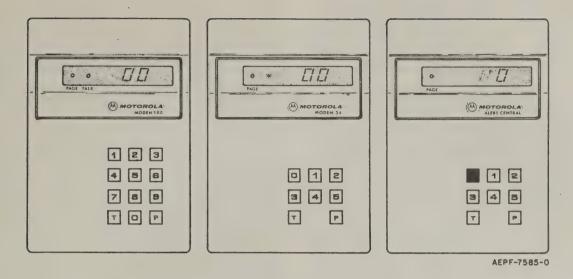


Figure 17. "Moden" Series Controls and Indicators

- (2) PAGE glows for the duration of the transmission of paging tones.
- (3) TALK glows for the duration of the voice transmission, available on "Moden" 100 only.

3. OPERATION

The following describes the operating procedure for each of the paging encoders described in this manual: "Moden" 100, "Moden" 36, and Alert Central. Refer to the applicable description for the paging encoder being used.

a. ''Moden'' 100 Paging Encoder Operation

Position the AC-OFF-DC power switch to the power source being used (AC or DC).

(1) Paging

- (a) Number Entry Enter the pager code number with the numbered pushbuttons on the keyboard. As a number is entered, it assumes the rightmost position and shifts to the left when another digit is entered (entry is from right to left). If a mistake is made in entering the pager code number, re-enter the correct code number.
- (b) Monitoring The channel must be monitored to prevent co-user interference, prior to depressing the P (page) or T (talk) pushbutton. This is accomplished by setting the receive audio

volume control on the base station in local control systems to a comfortable listening level. The transmitted message will be garbled if the channel is not clear. When clear, proceed to page or transmit.

NOTE

For carrier squelch systems - channel monitoring is automatic; i.e., the channel activity is heard when the base station is not transmitting.

For PL squelch systems - channel monitoring is accomplished by depressing the MONITOR switch on the microphone.

- (c) Tone-Only Paging When the P (page) keyboard pushbutton is momentarily depressed, an automatic paging cycle is initiated. The PAGE lamp glows, indicating that the transmitter is keyed and paging tones are being generated. While the PAGE lamp is on, the keyboard is locked out and no other function can be performed. At the end of the paging tone interval, the PAGE lamp goes out.
- (d) Tone-and-Voice Paging This operation is similar to a tone-only page with the following exceptions: after the PAGE lamp goes out (a new pager code number can then be entered), the TALK lamp begins to glow. At this time the voice message portion of the page should be given. The TALK lamp normally remains on for 8 to 10 seconds, but this time interval can be lengthened or shortened by depressing the T (talk) pushbutton on the keyboard or the TRANSMIT paddle on the microphone in carrier squelch systems. In a

PL squelch system, this is accomplished by depressing the T (talk) pushbutton on the keyboard only.

(2) Voice Transmission

To transmit a voice message without paging in a mixed mobile/paging system, use the following procedures:

- (a) Carrier Squelch System Monitor the channel as previously described. Depress and hold the TRANSMIT paddle on the microphone or the T (talk) pushbutton on the keyboard for the duration of the voice message.
- (b) PL Squelch System Monitor the channel as previously described. Simultaneously depress and hold the TRANSMIT and MONITOR paddles on the microphone for the duration of the voice message.

b. "Moden" 36 Paging Encoder Operation

Position the AC-OFF-DC power switch to the power source being used (AC or DC).

(1) Paging

- (a) Number Entry Enter the pager code number using the numbered pushbuttons on the keyboard. As a number is entered, it assumes the rightmost position and shifts to the left when another digit is entered (entry is from right to left). If a mistake is made in entering the pager code number, re-enter the correct code number.
- (b) Monitoring The channel must be monitored to prevent co-user interference, prior to depressing the P (page) or T (talk) pushbutton. This is accomplished by setting the receiver audio volume control on the base station in local control systems to a comfortable listening level. The transmitted message will be garbled if the channel is not clear. When clear, proceed to page or transmit.

NOTE

For carrier squelch systems - channel monitoring is automatic; i.e., the channel activity is heard when the base station is not transmitting.

For PL squelch systems - channel monitoring is accomplished by depressing the MONITOR switch on the microphone.

- (c) Tone-Only Paging When the P(page) keyboard pushbutton is momentarily depressed, an automatic paging cycle is initiated. The PAGE lamp glows, indicating that the transmitter is keyed and paging tones are being generated. While the PAGE lamp is on, the keyboard is locked out and no other function can be performed. At the end of the paging tone interval, the PAGE lamp goes out.
- (d) Tone-and-Voice Paging This operation is similar to a tone-only page with the following exceptions: BEFORE the PAGE lamp goes out, depress the T (talk) pushbutton on the keyboard or the TRANSMIT paddle on the microphone in carrier squelch systems. While holding the T (talk) pushbutton down, and after the PAGE lamp goes out, the voice message portion of the page should be given. In a PL squelch system, this is accomplished by depressing the T (talk) pushbutton on the keyboard.

(2) Voice Transmission

To transmit a voice message without paging in a mixed mobile/paging system, use the following procedures:

- (a) Carrier Squelch System Monitor the channel as previously described. Depress and hold the TRANSMIT paddle on the microphone or the T (talk) pushbutton on the keyboard for the duration of the voice message.
- (b) PL Squelch System Monitor the channel as previously described. Simultaneously depress and hold the TRANSMIT and MONITOR paddles on the microphone for the duration of the voice message.

c. Alert Central Paging Encoder Operation

Position the AC-OFF-DC power switch to the power source being used (AC or DC).

(1) Paging

(a) Monitoring - The channel must be monitored to prevent co-user interference, prior to depressing any of the numbered keyboard pushbuttons. This is accomplished by setting the receive audio volume control on the base station in local control systems to a comfortable listening level. The transmitted message will be garbled if the channel is not clear. When clear, proceed to page or transmit.

NOTE

For carrier squelch systems - channel monitoring is automatic; i.e., the channel activity is heard when the base station is not transmitting.

<u>For PL squelch systems</u> - channel monitoring is accomplished by depressing the MONITOR switch on the microphone.

(b) Number Entry and Tone-Only Paging - Enter the pager code number with the numbered pushbutton on the keyboard. As a number is entered, it is displayed and the automatic paging cycle is initiated. The PAGE lamp glows, indicating that the transmitter is keyed and paging tones are being generated. While the PAGE lamp is on, the keyboard is locked out and no other function can be performed. At the end of the paging tone interval, the PAGE lamp goes out.

NOTE

If the Alert Central paging encoder has been modified to disable the automatic paging function, depress the P (page) pushbutton to initiate the paging cycle.

(c) Group Call Entry and Tone-Only Paging - Depress the red pushbutton to initiate a group call page. When the red pushbutton is depressed, number zero will be displayed and the automatic paging cycle is initiated. The PAGE lamp glows, indicating that the transmitter is keyed and a group call paging tone is being

generated. While the PAGE lamp is on, the keyboard is locked out and no other function can be performed.

(d) Tone-and-Voice Paging - This operation is similar to a tone-only page with the following exceptions: BEFORE the PAGE lamp goes out, depress the T (talk) pushbutton on the keyboard or the TRANSMIT paddle on the microphone in carrier squelch systems. While holding the T (talk) pushbutton down and after the PAGE lamp goes out, the voice message portion of the page should be given. In a PL squelch system, this is accomplished by depressing the T (talk) pushbutton on the keyboard.

(2) Voice Transmission

To transmit a voice message without paging in a mixed mobile/paging system, use the following procedures:

- (a) Carrier Squelch System Monitor the channel as previously described. Depress and hold the TRANSMIT paddle on the microphone or the T (talk) pushbutton on the keyboard for the duration of the voice message.
- (b) PL Squelch System Monitor the channel as previously described. Simultaneously depress and hold the TRANSMIT and MONITOR paddles on the microphone for the duration of the voice message.

THEORY OF OPERATION

1. INTRODUCTION

Overall functions of the paging encoder are discussed first in general terms and then detailed circuit descriptions are given for each stage and its relationship to other stages within the paging encoder.

2. CIRCUIT DESCRIPTION

a. General

The paging encoder can be sectionalized into five functional sections: power supply, keyboard data entry, keyboard data display, paging tone frequency synthesizer, and timing and control circuits (see Figure 18).

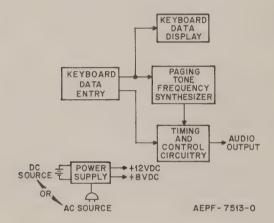


Figure 18. Paging Encoder Functional Sections

The power supply provides the power neccessary for the operation of the logic circuits, display LED, and relays. The keyboard data entry circuits encode the keyboard decimal input to binary-coded-decimal (BCD) information and supplies this binary information to the keyboard data display and the paging tone frequency synthesizer. The keyboard data display shows the decimal equivalent of the numbered button pushed on the keyboard. Also, it displays the page or talk mode. (The talk lamp is not part of the "Moden" 36 nor the Alert Central paging encoder.) The paging tone frequency synthesizer generates the paging tones equivalent to the input data from the keyboard. The timing and control circuitry uses inputs from the keyboard and synthesizer to control the paging tone timing period for an

individual call page, group call page, and to control the "Moden" 100 talk cycle. The timing and control circuitry also energizes the output relays so that the synthesizer paging tone can be sent to the base station for transmission. During the time the paging tone is being sent, the page lamp glows. At the end of the paging tone, the page lamp goes out and a voice message can be sent to the individual or group paged by depressing the keyboard talk pushbutton. On "Moden" 100 paging encoder, a talk lamp glows when a voice message can be sent (\$10 seconds). The talk pushbutton on the "Moden" 100 is held down to extend the talk time or if a shorter talk time is desired the talk pushbutton can be momentarily depressed. This resets the talk timer monostable.

Refer to the block diagram in Figure 19 and the schematic diagram for the following descriptions.

b. Power Supply

The paging encoder operates from either a 117-volt ac source, a 234-volt ac source, or a 12-18-volt dc source. The input voltage is applied through a full-wave rectifier before being applied to the +8-volt dc and +12-volt dc regulators.

The dc input power, when used, is applied directly to the +8-volt dc and +12-volt dc regulator circuits.

The output voltage from the +12-volt dc regulator is used to energize the output relays, and the +8 volts dc from the +8-volt regulator is used to energize the logic circuitry and LED display lamps.

c. Keyboard Data Entry Circuitry

Keyboard decimal digits (1, 2, 3, etc.) are encoded by decimal-to-binary keyboard encoder U2 to produce a binary coded decimal (BCD) input to parallel input keyboard data storage registers B (U3 and U5), and A (U4 and U6).

The first digit entered into the keyboard is entered into register B in parallel form by the load/transfer pulse generated by keyboard strobe and debounce circuit U7D. The second digit entered into the keyboard is entered into register B in the same manner as the first digit, and the first digit is simultaneously transferred into register A.

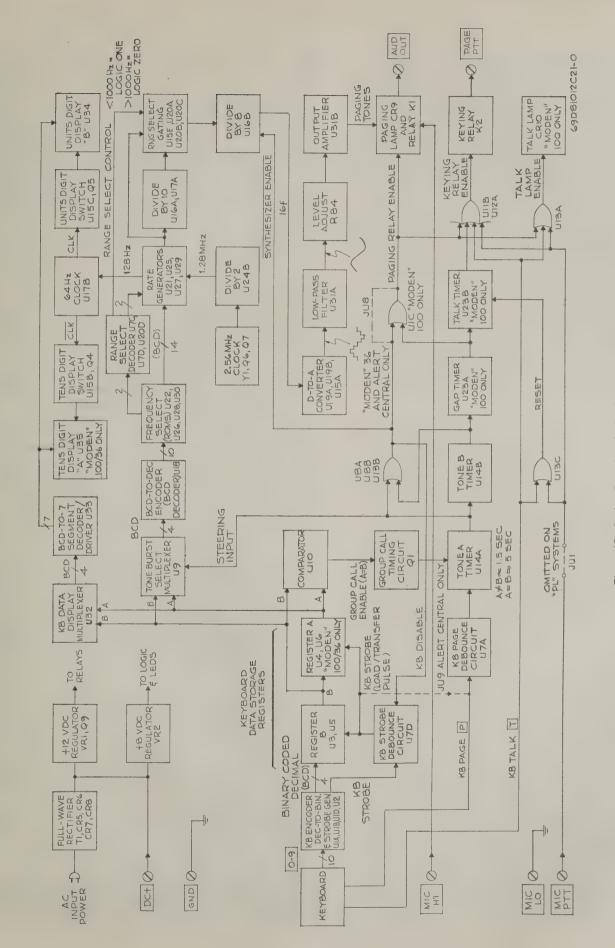


Figure 19. Paging Encoder Block Diagram

d. Keyboard Data Display

The digits entered into the keyboard appear in BCD format at the output of registers U3, U4, U5, and U6. The most significant digit (tens) appears at the output of register A (U4 and U6) and the least significant digit (units) appears at the output of register B (U3 and U5). This data is applied to the input of keyboard data display multiplexer U32 in parallel form.

The BCD output of the keyboard data display multiplexer drives BCD-to-seven decoder/driver U33 to provide a decimal readout on tens digit display A and on units digit display B.

The digital display readout is controlled by the 64 Hz clock from U17B. The 64 Hz clock produces a two-line select output: CLK and $\overline{\text{CLK}}$. The $\overline{\text{CLK}}$ and CLK outputs are fed respectively to tens digit display switch U15B and Q4 and to units digit display switch U15C and Q5 to provide an alternating ground signal to light the digital display LED's one at a time.

e. Paging Tone Frequency Synthesizer

The outputs of keyboard data storage registers A and B are applied to the input of tone burst select multiplexer U9. The tone burst select multiplexer applies the outputs of registers A and B to BCD-to-decimal encoder U18, one register at a time; register A first and then register B. This action is controlled by the timing and control circuits described in paragraph 2.f. of this section. The BCD-to-decimal encoder provides a decimal equivalent (0-9) of the register being sampled to the address inputs of frequency select read-only memories (ROM's) U22, U26, U28, and U30.

Tone generation is accomplished primarily by rate generators U21, U25, U27, and U29 with the tone frequency being selected by BCD outputs of frequency select ROM's U22, U26, U28, and U30. Each of the rate generators receives a BCD input from the frequency select ROM's that determines the number of pulses the rate generator will produce from every ten thousand clock pulses applied. The principle involved is that of adding pulses at predetermined intervals such that the number of pulses produced for every ten thousand clock pulses equals the desired output tone frequency times 128 (2.56 MHz clock frequency divided by 2 and then divided by 10,000 = 128f). This method does not produce a train of equally spaced pulses; it yields only the proper number from every ten thousand clock pulses.

The output of the rate generator is routed to the input of both the divide-by-10 circuit, U17A and Ul6A, and the range select gating circuit, U15E, U20A, U20B, and U20C. If the tone frequency is to be less than 1000 Hz, the range select control output of range select decoder U20D is a logic "one." This disables the bypass function of the range select gating circuit and applies the output of the divide-by-10 circuit to the input of the divide-by-8 circuit. Conversely, if the tone frequency is to be greater than 1000 Hz, the range select control output of the range select decoder is a logic "zero." This enables the bypass function of the range select gating circuit and applies the output of the rate generator directly to the input of the divide-by-8 circuit. This action changes the final output frequency by a factor of ten: therefore, at frequencies less than 1 kHz .1 Hz accuracy is obtained and 1 Hz accuracy for frequencies greater than 1 kHz.

The output of divide-by-8 circuit U16B is routed to digital-to-analog converter U19A, U19B, and U15A when the timing and control circuit initiates the synthesizer enable signal. This circuit produces a raised voltage output for eight clock pulses and a falling voltage output for the next eight pulses applied. The output of the digital-to-analog converter is a stepped waveform resembling a sine wave. Sixteen clock pulses are required to produce one full cycle of the digital-to-analog converter output.

The output of digital-to-analog converter U19A, U19B, and U15A is coupled through low-pass filter U31A, which shapes the stepped output of the digital-to-analog converter into a near perfect sine wave, through level adjust R84, to the input of output amplifier U31B. The output of the amplifier is coupled through paging relay K1 (when energized) to the audio output screw terminal.

f. Timing and Control Circuits

For the "Moden" 36 and "Moden" 100 paging encoders, after the paging call code has been entered into the keyboard and before the keyboard page pushbutton is depressed, timing and control circuit comparator U10 compares digit A against digit B from the keyboard data storage registers. If digits A and B are not the same, the comparator output does not change and the tone A timing constant of tone A timer U14A is not affected. If digits A and B are the same, the comparator output feeds a group call enable signal to group call timing circuit Q1 to elongate the tone A timing constant. Depressing the page pushbutton initiates

the circuitry required to enable the transmitter, initiates the appropriate timing cycles, and enables the generation of the appropriate encoder tones.

For the Alert Central paging encoder, after the paging call code or group call code (red pushbutton) is entered into the keyboard, the keyboard strobe load/transfer pulse, simultaneously, loads the paging call code digit into register B and, via jumper JU9, pulses the page input to keyboard page debounce circuit U7A. This automatic paging function initiates the circuitry required to enable the transmitter, initiates the appropriate timing cycles, and enables the generation of the appropriate encoder tones.

In the "Moden" 36 and "Moden" 100 paging encoders, the keyboard page signal is fed through keyboard page debounce circuit U7A to produce a clean strobe to prevent triggering the tone A timer more than once for each timing cycle. The Alert Central page signal comes from the keyboard strobe load/transfer pulse and is also fed through the keyboard page debounce circuit to produce a clean strobe to trigger the tone A timer.

When tone A timer Ul4A timing is initiated, several stages are enabled. First, the tone A timer enables the tone burst select multiplexer to sample keyboard data storage register A. The same enabling signal is fed through OR gates U13B, U8A, and U8B to produce the synthesizer enable input signal to divide-by-8 U16B and paging relay gate UIC (jumper JU8 replaces UIC in the "Moden" 36 and the Alert Central paging encoders). The output of OR gate U13B also produces the keyboard disable input signal which disables the keyboard from accepting more paging codes while paging. The divide-by-8 circuit being enabled routes the tone A paging tone to the paging relay contact. The synthesizer enable at the input of paging relay gate UIC (jumper JU8 in "Moden" 36 and Alert Central paging encoders) is fed through to energize paging relay Kl, to energize keying relay K2, and to turn on paging lamp CR9. Energizing paging relay K1 connects the synthesizer paging tones from output amplifier U31B to the audio output screw terminal for transmission by a base station. Energizing keying relay K2 provides a switched ground to the base station for keying purposes.

At the termination of the tone A timer, tone B timer U14B is initiated and the signal level to U9 select inputs is changed which causes the tone burst select multiplexer to sample keyboard data storage register B. Tone B timer maintains relays K1 and K2 energized for its duration, allowing the transmission of the tone B paging tone from the paging tone frequency synthesizer. It also continues to disable the keyboard and enable the synthesizer.

For the "Moden" 36 and the Alert Central paging encoders, if a voice message is to be sent, the keyboard talk pushbutton must be depressed before the page lamp goes out (tone B terminated). By depressing the keyboard talk pushbutton, keying relay K2 is kept energized through keying relay gate UllB and Ul2A while the paging relay and lamp are de-energized when the tone B timer terminates. A voice message can be given as long as the keyboard talk pushbutton is depressed.

When the "Moden" 100 paging encoder tone timer B terminates, gates U13B, U8A, and U8B remove the synthesizer enable signal from the divide-by-8 input so that paging tones will no longer be generated. It also removes the keyboard disable signal to enable the keyboard to accept a new paging code. The enabling pulse to the input of paging relay gate U1C is removed when the tone B timer terminates, but at the same time, when gap timer U23A is initiated, another enabling pulse is routed to the input of paging relay gate U1C to maintain the paging and keying relays and the paging LED energized.

The gap timer provides a gap or space between the paging tones and the voice message to allow the paging receiver to enable its audio circuitry to receive a voice message after receiving tone B.

At the end of the gap timer timing cycle, relay K1 is de-energized, paging lamp CR9 goes out, the audio output switches from the paging tone input to the microphone audio input, talk timer U23B is initiated to maintain keying relay K2 in its energized condition, and talk lamp CR10 begins to glow. The talk time is nominally 10 seconds for sending a voice message.

If no voice message is sent, another paging code can be entered into the keyboard data storage registers and another page initiated by depressing the page pushbutton. This resets the talk timer and starts the tone timing over again.

The talk timer timing cycle can be shortened by momentarily depressing ("flashing") the keyboard talk pushbutton or the microphone push-totalk paddle.

A voice message, not preceded by a paging tone, can be transmitted by depressing the keyboard talk pushbutton or microphone push-to-talk paddle. This energizes keying relay K2 through keying relay enable gate U12A which will key the base station transmitter. Relay K1 is in the de-energized state and therefore, microphone audio is routed through to the base station. The talk lamp is energized through talk lamp enable gate U13A.

MAINTENANCE

1. INTRODUCTION

This section describes recommended repair procedures, special precautions regarding maintenance, recommended test equipment, and system troubleshooting techniques. Each of these topics provides information vital to the successful operation and maintenance of the "Moden" Series Paging Encoders described in this manual.

2. PREVENTIVE MAINTENANCE

a. Visual Inspection

Check that external surfaces of the equipment are clean, that connecting cables and wires are not damaged, and that connections are firm. A detailed inspection of the interior electronic circuits is not needed or desired.

b. Cleaning

Periodically clean smudges and grime from the exterior of the housing. Use a soft, nonabrasive cloth <u>moistened</u> in a mild soap and water solution. Rinse the surface using a second cloth <u>moistened</u> in clean water.

3. DISASSEMBLY

The "Moden" Series Paging Encoder described in this manual can be disassembled to where the circuit boards are exposed or to where the circuit boards are completely removed from the housing. Disassemble the paging encoder as follows:

a. Housing Top Removal

- (1) Disconnect the paging encoder from its power source.
- (2) From the bottom of the housing, remove four screws; refer to Figure 2 for the screw locations.

NOTE

The paging encoder housing (top and bottom) is interconnected by the display circuit board cable.

(3) Carefully remove the top of the housing, and disconnect the keyboard cable from the main circuit board. Refer to Figure 20.

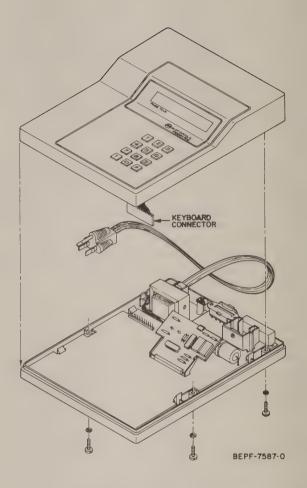


Figure 20. Housing Top Removal

b. Display Circuit Board Removal

- (1) Disengage the spring retaining clip from the top edge of the display circuit board. Refer to Figure 21.
- (2) Grasp the display circuit board holder as shown in Figure 21. Use the thumbs to push on the sides of the circuit board holder to disengage its locking device.
- (3) When the locking device is free from the circuit board and while still applying pressure with the thumbs, use the index fingers to raise the circuit board slightly above the locking device of the circuit board holder.

(4) Grasp the top edge of the circuit board and "walk" or wiggle the circuit board out from its connector.



Figure 21.
Display Circuit Board Removal

c. Main Circuit Board Removal

(1) The main circuit board is held in place by four plastic clips. Refer to Figure 22 and follow the steps illustrated for all four circuit board clips.

NOTE

The power transformer is hard-wired to the main circuit board.

- (2) Carefully lift the main circuit board to expose the solder side of the board.
- (3) To completely remove the main circuit board, unsolder five wires from the circuit board; three are located to the left of the display circuit board connector (viewed from component side) and two are located near the fuse and power switch. Refer to the "Circuit Board Detail."

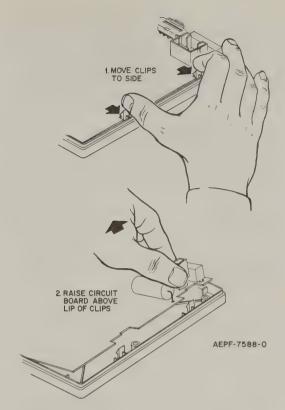


Figure 22. Main Circuit Board Removal

4. TROUBLESHOOTING

Servicing of the paging encoder requires the localizing of the malfunctioning circuit before the defective component can be isolated and replaced. Since localizing and isolating a defective component constitutes the most time-consuming part of troubleshooting, a thorough understanding of the circuits involved will aid the technician in performing efficient servicing. The technician must know how one function affects another; he must be familiar with the overall operation of the encoder and the procedures necessary to place it back in operation in the shortest possible time.

The paging encoder functional diagrams, schematic diagrams, and troubleshooting charts (Figures 23 through 34) provide valuable information for troubleshooting purposes. The functional diagram provides signal flow information in a simplified format while the schematic diagram provides the detailed circuitry and the biasing voltages required for isolating malfunctioning components. The troubleshooting charts further isolate malfunctioning components. Generally, it may be assumed that if the paging encoder is totally inoperative, the power inputs or power supply is defective. However, if the paging encoder operates in the transmit mode but

not in the receive mode (or vice versa), it may be assumed that the power supplies are serviceable and that one or more functional circuits are defective or marginal. By using the diagrams, troubleshooting charts, and deductive processes, the suspected circuit may be readily found.

5. RECOMMENDED TEST EQUIPMENT

Service Monitor - Motorola Model S-1327B

Oscilloscope, Dual Trace - Telequipment Model D67 or equivalent.

Digital Multimeter - Motorola Model T-1048A or equivalent.

VOM - Motorola Model ST-1089

Audio Oscillator - Motorola Model S-1067B or equivalent.

Frequency Counter - Motorola Model S-1343A or equivalent.

AC Voltmeter - Motorola Model S-1053C or equivalent.

Miniature Soldering Iron - Motorola ST-916 or equivalent.

6. MOS HANDLING PRECAUTIONS

MOS (Metal Oxide Semiconductor) devices are used in the paging encoder. While the attributes of MOS type devices are many, their characteristics make them susceptible to damage by electrostatic or high voltage charges. Therefore, when the service technician encounters MOS circuits, special precautions to prevent device damage must be taken during repair procedures outlined in the following sections. The following handling precautions are recommended for MOS circuits and are especially true in dry-humidity conditions.

- a. Store and transport all MOS devices in conductive material so that all exposed leads are shorted together. Do not insert MOS devices into conventional plastic "snow" or plastic trays of the type used for storage and transportation of other semiconductor devices.
- b. Ground the working surface of the service bench to protect the MOS device.

- c. Wear a conductive wrist strap in series with a 100 k resistor to ground.
- d. Do not wear nylon clothing while handling MOS devices.
- e. Neither insert nor remove MOS devices with power applied. Check all power supplies to be used for testing MOS devices and be certain there are no voltage transients present.
- f. When straightening MOS leads, provide ground straps for apparatus used.
- g. When soldering, use a grounded soldering iron.
- h. If at all possible, handle all MOS devices by the packages and not by the leads. Prior to touching the unit, touch an electrical ground to remove any static charge that you may have accumulated. The package and substrate may be electrically common. If so, the reaction of a discharge to the case would cause the same damage as touching the leads.

7. REPAIR PROCEDURES

a. Parts and Substitution

When damaged parts must be replaced, identical parts should be used. If the identical replacement component is not locally available, check the parts list of the respective printed circuit board for the proper Motorola part number and order the components from the nearest Motorola Replacement Parts Depot as listed in the "Replacement Parts Ordering" section of this instruction manual. If for any reason substitutions must be made immediately, it is recommended that the substitutions be replaced as soon as the proper replacement part is available. The substituted part must have identical electrical properties and must be of equal or higher voltage and current ratings.

b. Component Removal

Most components are located on circuit boards. Special care should be taken during troubleshooting to be as certain as possible that the suspected component is actually the one at fault. The special care will eliminate unnecessary unsoldering and removal of parts which may damage or weaken other components or the circuit board itself.

CAUTION

MOS integrated circuits are used extensively throughout the system; use special care when handling these devices. See "MOS Handling Precautions" paragraph in this section.

Use of a 40-watt pencil type soldering iron is recommended. The Motorola ST-639 Printed Circuit Repair Kit contains a recommended 40-watt iron as well as soldering aids (probers), magnifying glass, solder, solvent, and brush. A solder remover of the squeeze-bulb type such as the ST-726 is also recommended. Use an iron with a tapered point to permit its exact application to the desired connection in compact equipment. Always keep the soldering iron tip well tinned and clean.

c. Soldering

Before soldering any connections, carefully scrape all parts to be soldered until all traces of rust, corrosion, paint or varnish are removed. Dust the scraped parts with a small clean brush. Tin all surfaces to be soldered. Wrap the wire around the lug to be soldered to obtain sufficient mechanical support (if applicable). Solder the connection, using a minimum amount of solder with sufficient heat to make the solder flow evenly around the tinned surface.

d. Printed Circuit Repair Techniques

Using a soldering iron with low heat output, in many cases, has actually caused damage that the serviceman was trying to prevent while repairing printed circuits. It is absolutely necessary to raise the temperature of the connection until the solder flows freely around the board eyelet. This usually takes a considerable amount of time with a very low heat iron. During this time heat is conducted away from the connection by the printed wiring causing it, in some instances, to break away from the board. If a component is to be removed, its soldered connections must be raised to a temperature that permits free flow of solder. Otherwise the component leads may not be freed from the printed wiring and the wiring will be pulled loose from the board as the component is removed. The soldering iron supplied with the Motorola Printed Circuit Repair Kit is

recommended for most work on printed circuit boards. This high-heat iron need be applied only a very short time to heat a connection to the point where solder flows freely. It is obvious that an iron this hot should not be held on a connection longer than necessary. Extended periods of high heat will cause the foil to peel loose from the board.

Breaks in the printed circuit wiring can be repaired by bridging the gap with solder. Remove the resin coating covering the printed wiring with solvent before soldering. Large areas of the printed wiring that have peeled loose can be repaired with a piece of hook-up wire. The hook-up wire should follow along the path of the original printed wiring. This avoids any lead dressing problem in critical circuits.

When removing resistors, capacitors and similar components, heat the connection to be loosened until the solder is molten. Then remove as much of the molten solder as possible. If the leads are bent over, use a soldering aid tool or a knife to straighten them. It may be necessary to apply the soldering iron while doing this. While applying the soldering iron, wiggle the component lightly to free it. Then lift it from the circuit board. Be sure the component leads are free before trying to remove them or you might pull loose some of the printed circuit wiring. Clean the circuit wiring around the holes with solvent. Install the new component and solder it in place. Coat the cleaned area of the circuit board with silicon resin. Such a coating seals the board from excessive moisture, prevents corrosion of the copper pattern, helps maintain insulation resistance and improves the appearance of the work. Never let solder flux bridge the gaps between the wiring pattern. This can reduce the resistance between circuits to only a few megohms which will cause leakage and disrupt certain electronic circuits. Use solvents to clean away flux after soldering. Defective components can also be replaced by clipping the leads as close to the component as possible. Solder the replacement component to these leads. Caution should be used when applying heat so that the original leads don't fall out of the board. This method of component replacement should not be used if the equipment is subjected to severe vibration.



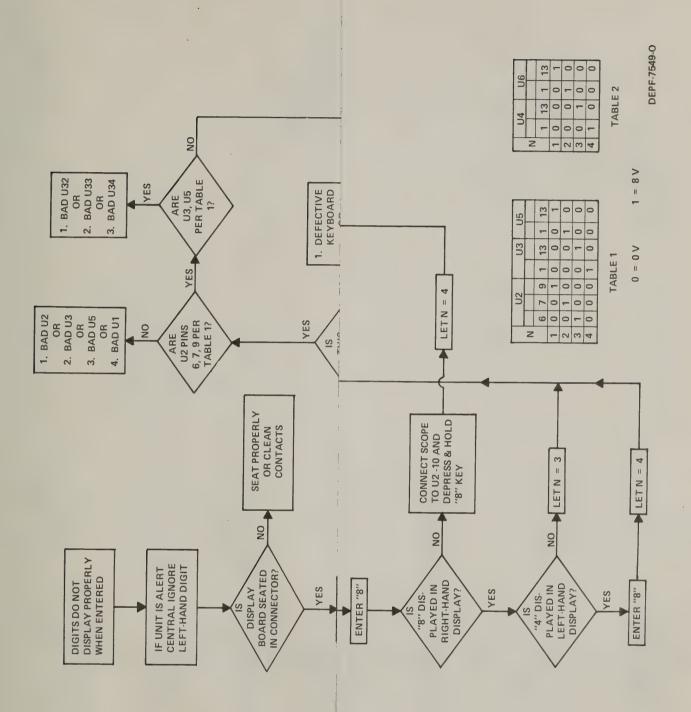


Figure 23.
"Digits Do Not Display Properly When Entered"
Troubleshooting Chart



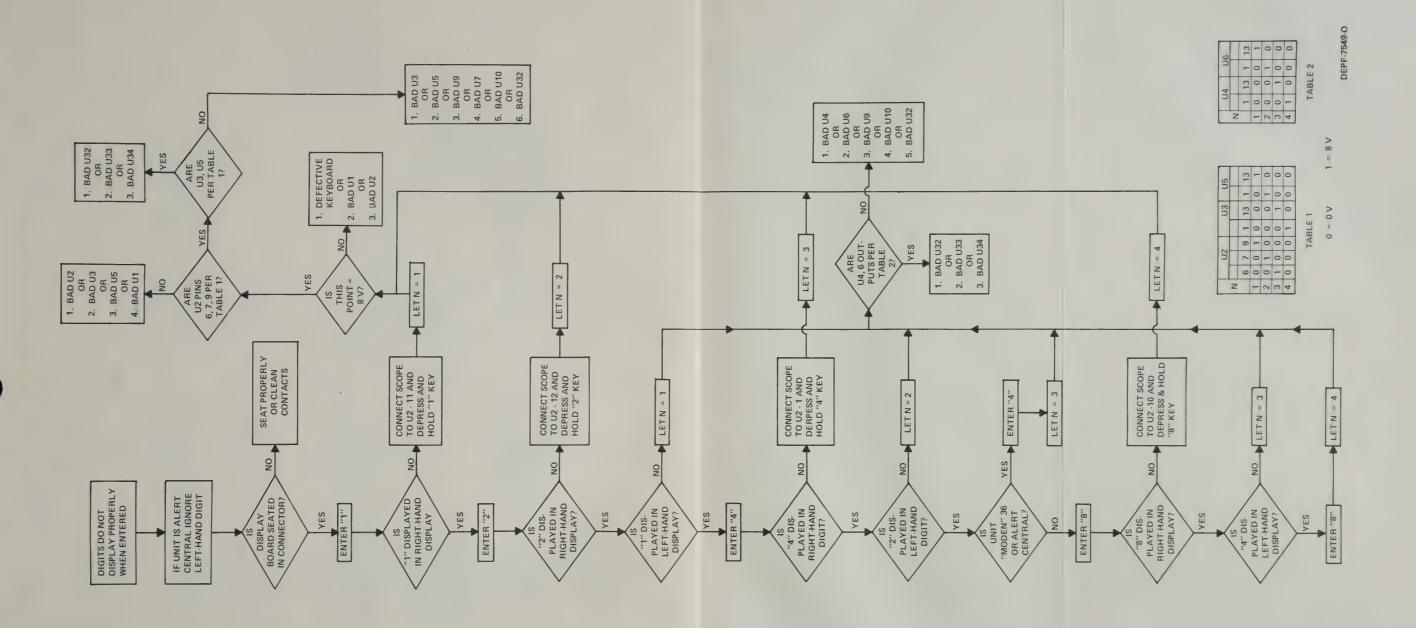


Figure 23.
"Digits Do Not Display Properly When Entered"
Troubleshooting Chart

Figure 24. "Unit Will Not Page Pager" Troubleshooting Chart

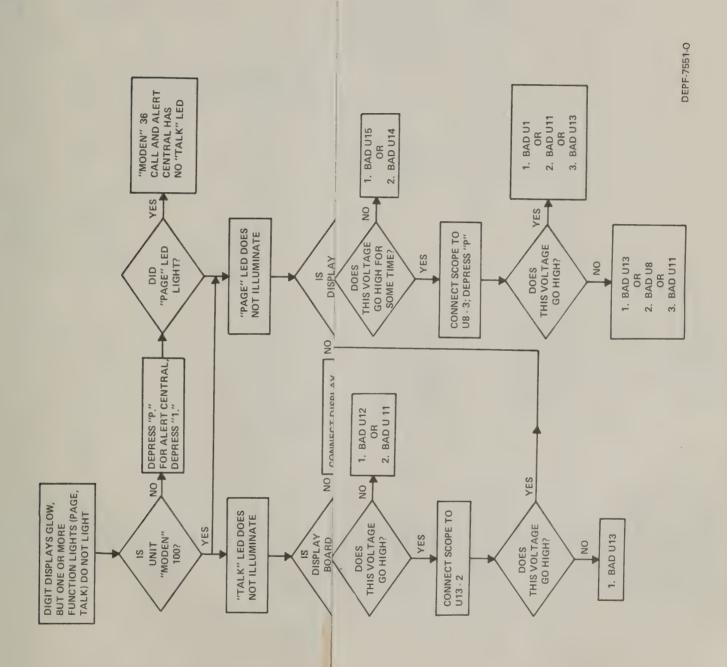


Figure 25.
"Digit Displays Glow, But One Or More Function Lights (PAGE, TALK) Do Not Light"
Troubleshooting Chart

Figure 24. "Unit Will Not Page Pager" Troubleshooting Chart

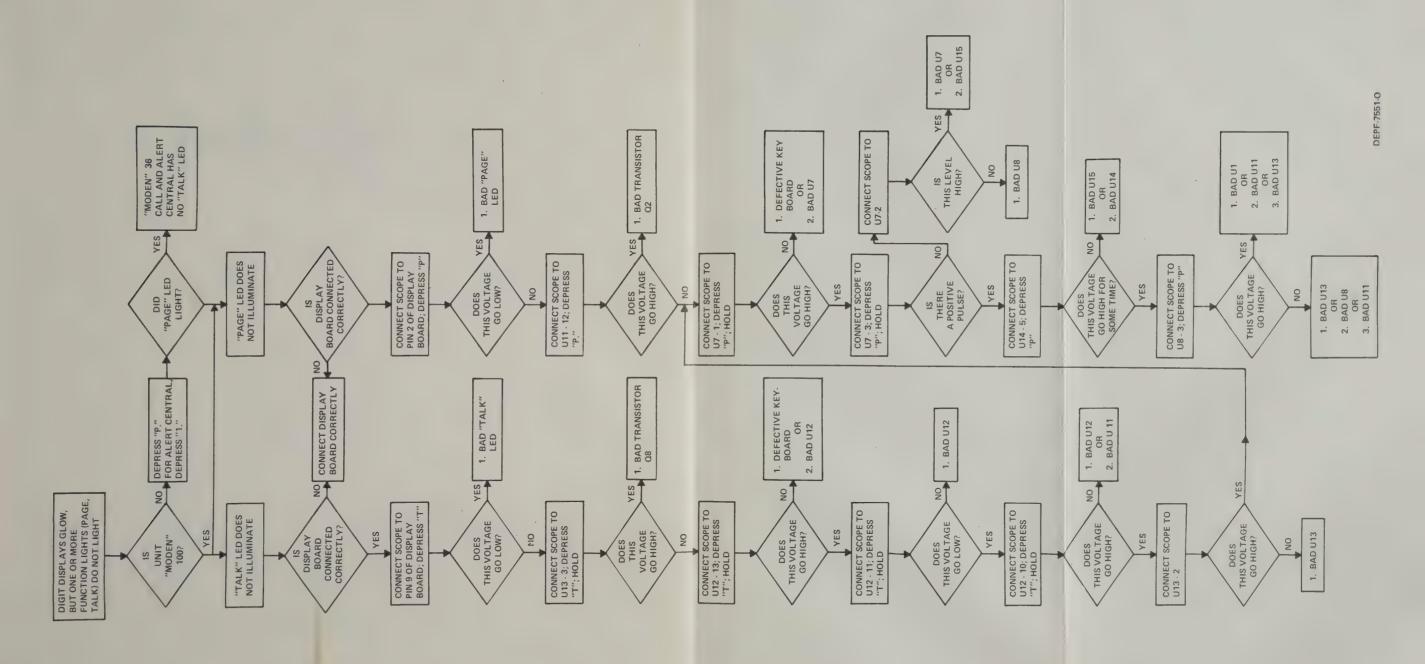


Figure 25.
"Digit Displays Glow, But One Or More Function
Lights (PAGE, TALK) Do Not Light"
Troubleshooting Chart

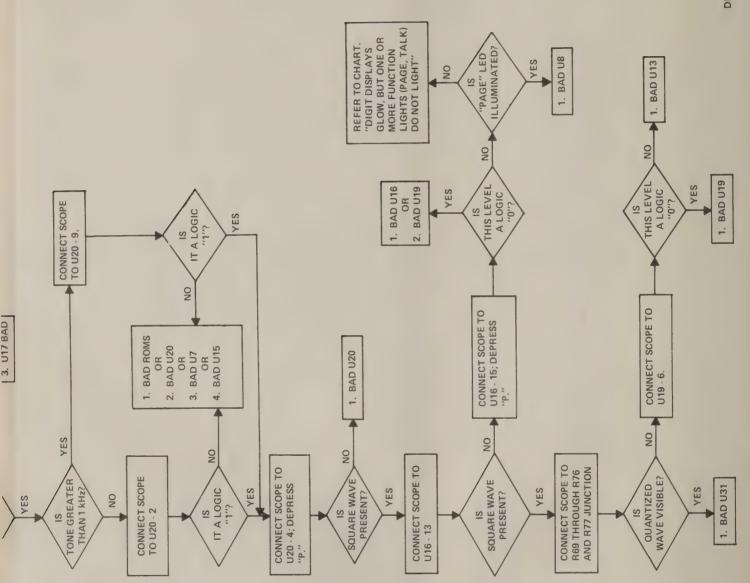


Figure 26.
"Transmitter Keys; Voice Present, But No Paging Tones"
Troubleshooting Chart

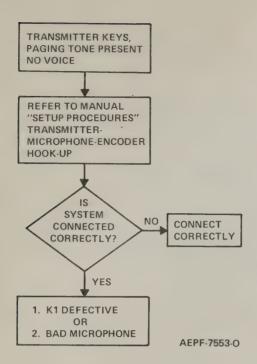


Figure 27.
"Transmitter Keys;
Paging Tone Present, But No Voice"
Troubleshooting Chart

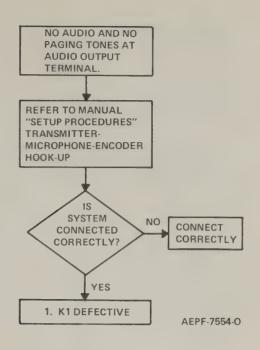


Figure 28.
"No Audio and No Paging Tones at
Audio Output Terminal"
Troubleshooting Chart

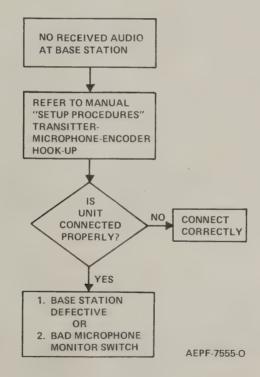


Figure 29.
"No Received Audio at Base Station"
Troubleshooting Chart

Figure 26.
"Transmitter Keys; Voice Present, But No Paging Tones"
Troubleshooting Chart

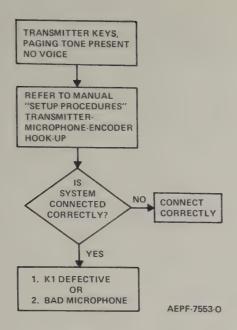


Figure 27.
"Transmitter Keys;
Paging Tone Present, But No Voice"
Troubleshooting Chart

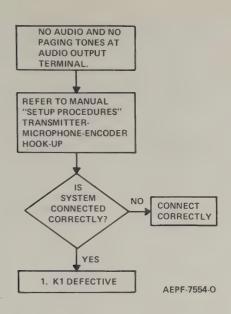


Figure 28.
"No Audio and No Paging Tones at
Audio Output Terminal"
Troubleshooting Chart

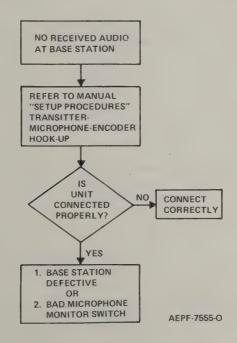


Figure 29.
"No Received Audio at Base Station"
Troubleshooting Chart

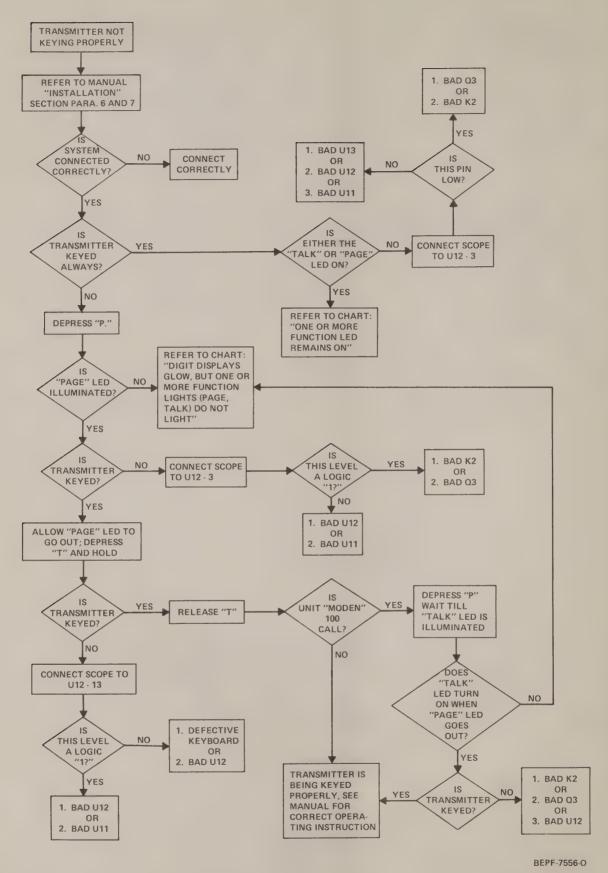


Figure 30.
"Transmitter Not Keying Properly"
Troubleshooting Chart

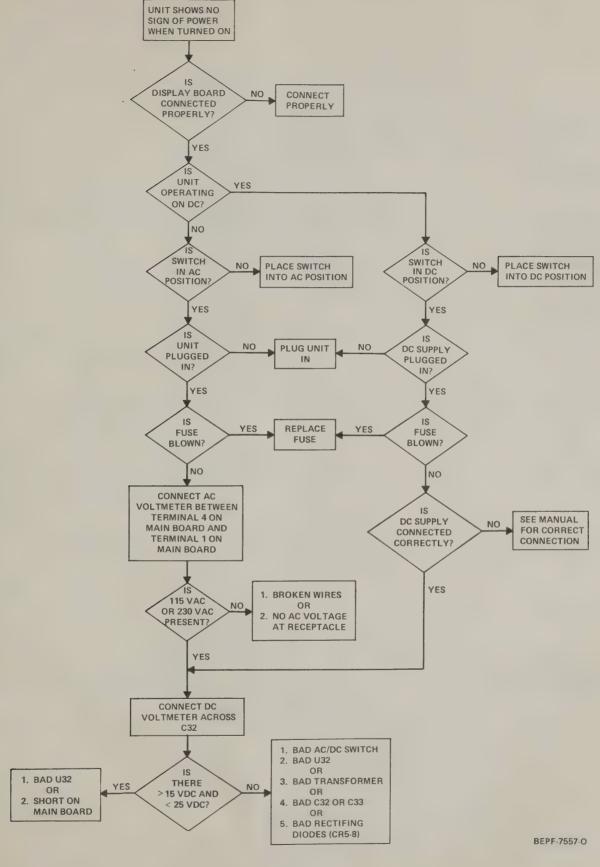


Figure 31.
"Unit Shows No Sign of Power When Turned On"
Troubleshooting Chart

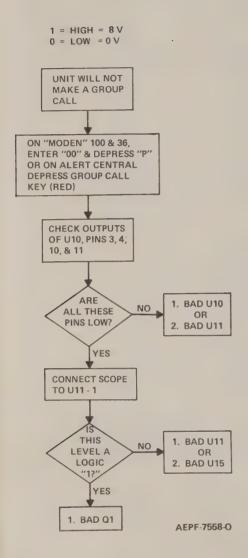


Figure 32. "Unit Will Not Make a Group Call Page" Troubleshooting Chart

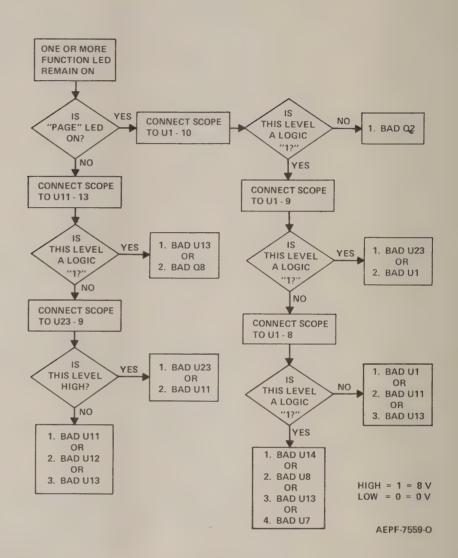


Figure 33.
"One or More Function LED Remains On"
Troubleshooting Chart

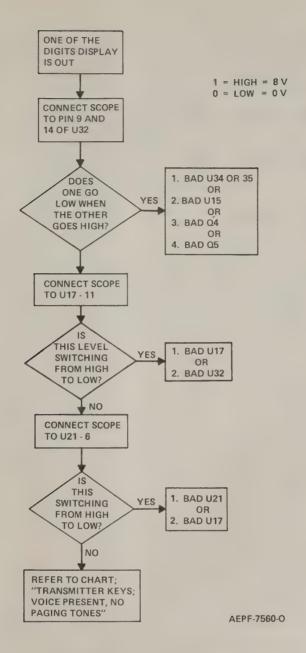
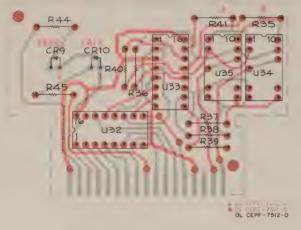


Figure 34.
"One of the Digits Display is Out"
Troubleshooting Chart

DISPLAY CIRCUIT BOARD

VIEWED FROM COMPONENT SIDE



DISPLAY CIRCUIT BOARD COMPONENT USAGE

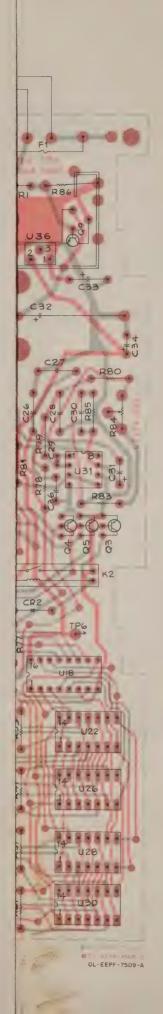
	PAGING ENCODER			
REF. DES.	"MODEN"	"MODEN" 36	"MODEN" ALERT CENTRAL	
CR10 R45 U35	USED USED USED	NOT USED NOT USED USED	NOT USED NOT USED NOT USED	

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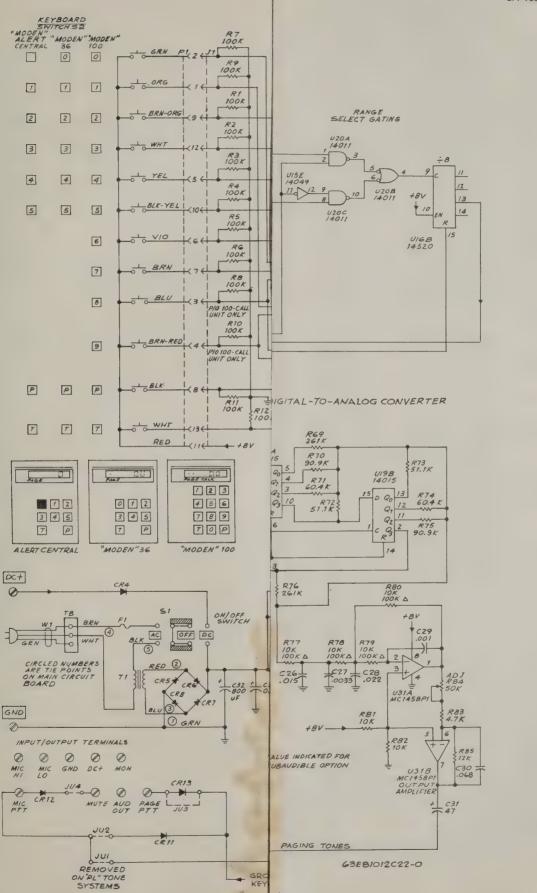
MAIN CIRCUIT BOARD COMPONENT USAGE

REF.		PAGING ENCODER	
DES.	"MODEN"	"MODEN"	ALERT
DEG.	100	36	CENTRAL
C12	USED	NOT USED	NOT USED
C13	USED	NOT USED	NOT USED
C14	USED	NOT USED	NOT USED
C15	USED	NOT USED	NOT USED
C16	USED	NOT USED	NOT USED
C17	USED	NOT USED	NOT USED
Q4	USED	USED	NOT USED
O8	USED	NOT USED	NOT USED
R8	USED	NOT USED	NOT USED
R10	USED	NOT USED	NOT USED
R22	USED	NOT USED	NOT USED
R28	USED	NOT USED	NOT USED
R29	USED	NOT USED	NOT USED
R30	USED	NOT USED	NOT USED
R31	USED	NOT USED	NOT USED
R42	USED	USED	NOT USED
U1	USED	NOT USED	NOT USED
U4	USED	USED	NOT USED
U6	USED	USED	NOT USED
U23	USED	NOT USED	NOT USED
U26	USED	NOT USED	NOT USED
U30	USED	NOT USED	NOT USED

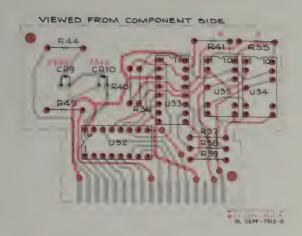
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EPF-7506-0



MAIN CIRCUIT BOARD



DISPLAY CIRCUIT BOARD COMPONENT USAGE

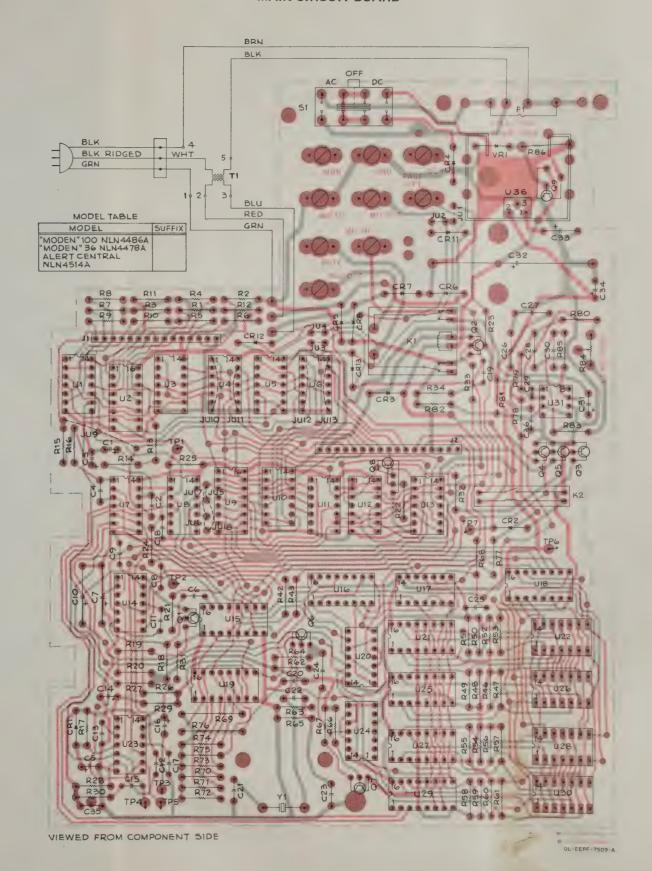
		PAGING ENCODER	}
REF. DES.	"MODEN"	"MODEN" 36	"MODEN" ALERT CENTRAL
CR10 R45 U35	USED USED USED	NOT USED NOT USED USED	NOT USED NOT USED NOT USED

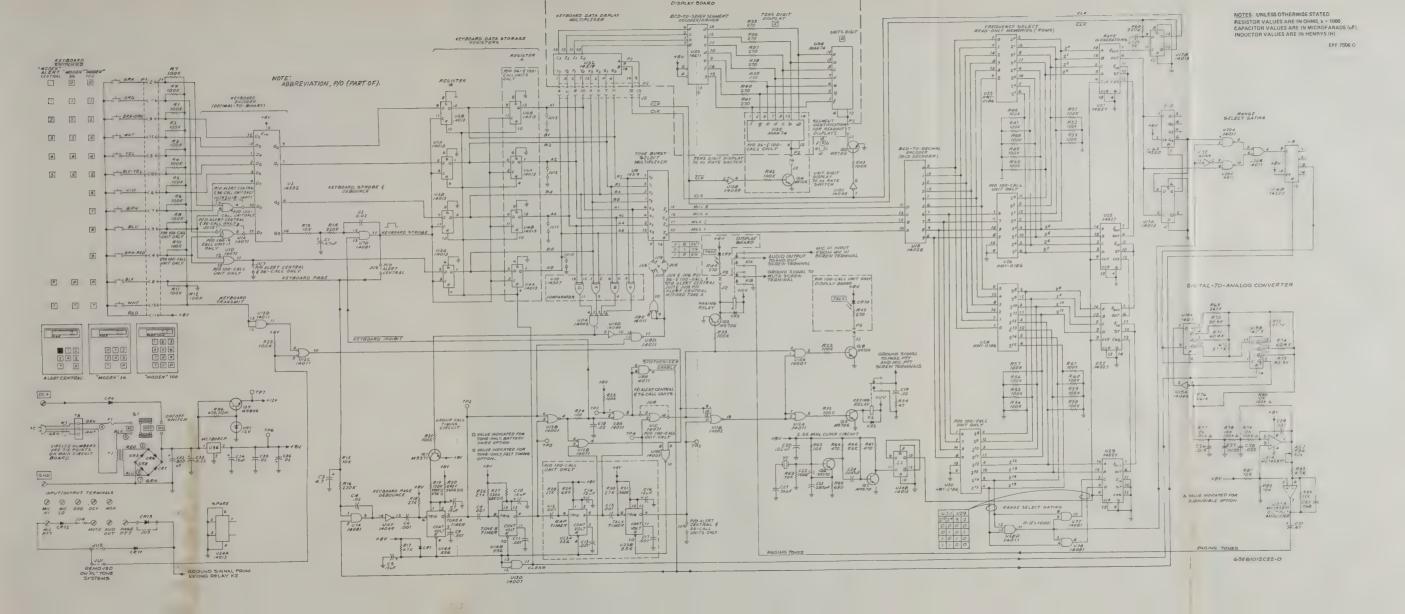
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MAIN CIRCUIT BOARD COMPONENT USAGE

0.55		PAGING ENCODER			
REF.	"MODEN"	"MODEN"	ALERT		
DES.	100	36	CENTRAL		
C12	USED	NOT USED	NOT USED		
C13	USED	NOT USED	NOT USED		
C14	USED	NOT USED	NOT USED		
C15	USED	NOT USED	NOT USED		
C16	USED	NOT USED	NOT USED		
C17	USED	NOT USED	NOT USED		
04	USED	USED	NOT USED		
0.8	USED	NOT USED	NOT USED		
R8	USED	NOT USED	NOT USED		
R10	USED	NOT USED	NOT USED		
R22	USED	NOT USED	NOT USED		
R28	USED	NOT USED	NOT USED		
R29	USED	NOT USED	NOT USED		
R30	USED	NOT USED	NOT USED		
R31	USED	NOT USED	NOT USED		
R42	USED	USED	NOT USED		
U1	USED	NOT USED	NOT USED		
U4	USED	USED	NOT USED		
U6	USED	USED	NOT USED		
U23	USED	NOT USED	NOT USED		
U26	USED	NOT USED	NOT USED		
U30	USED	NOT USED	NOT USED		

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APPENDIX A GLOSSARY

CODE TYPE - pager coding method requiring a prefix letter for each code.

KEY (transmitter) - process of activating the base station transmitter for the purpose of producing rf energy.

LOCAL (transmitter) - transmitter (base station) located at the same site as the encoder.

"PRIVATE-LINE" (PL) - method of implementing private (or semi-private) communications using a coded PL tone to unsquelch the receiver.

ROM - Read-Only Memory; integrated circuit packages used to store two-tone frequency information.

REMOTE (transmitter) - transmitter located at a remote site and interconnected with the encoder through a remote control console.

SUBAUDIBLE PAGING TONES - audio paging tones in the frequency range below the band-pass of most communications receivers (below 300 Hz).

SYNTHESIZER - a device which generates many output frequencies based on a single stable frequency source. The divider type uses a crystal-controlled master oscillator and outputs are submultiples of the master oscillator.

TWO-TONE SYSTEM - paging system based on two distinct paging frequencies.

NLN4486A Moden 100 NLN4478A Moden 36 NLN4514A Alert Central

PLF-1178-0

NLN4514A A	lert Central	PLF-1178-0
REFERENCE	MOTOROLA	
SYMBOL	PART NO.	DESCRIPTION
OTHIDOL	1101	
		CAPACITOR, Fixed: pF ± 5%
		100 V unless stated
Cl	2383441B18	4 7 120% 20 V
C2	2181428B18	4.7 uF +20%; 20 V .02 uF-40 +60%
		.02 UF -40 +60%
C3	2383441B18	4.7 uF +20%; 20 V .02 uF-40 +60%
C4	2182428B18	.02 uF-40 +60%
C5	2383441B26	15 uF +20%; 20 V
C6	2182187B20	15 uF +20%; 20 V 1000 +10%; 200 V
C7	2382783B24	15 uF; 25 V 1000 ±10%; 200 V 15 uF; 25 V
C8, 9' .	2182187B20	1000 <u>+</u> 10%; 200 V
C10	2382783B24	15 uF; 25 V
C11, 12, 13	2182187B20	1 1000 +10%: 200 V
C14	2383441B26	15 uF +20%; 20 V
C15	2182187B20	
C16	2383441B26	1000 ±10%: 200 V 15 uF ±20%; 20 V 1000 ±10%; 200 V .02 uF -40 +60% 36; 500 V
C17	2182187B20	1000 +10%; 200 V
C18, 19, 20	2182428B18	.02 uF -40 +60%
C21	2184426B16	36: 500 V
C22	2184426B63	1500
C23	2184426B54	280: 500 V
C24	0882905G26	280; 500 V .0047 uF .02 uF -40 +60%
C25	2182428B18	.02 uF -40 +60%
C26	0882905G10	015 nF: 50 V
C25	0882905G10 0882905G25	.015 uF; 50 V .0033 uF
		033 42
C28	0882905G02	.022; 50 V
C29	2182213E08	1000
C30	0882905G04	.068 uF; 50 V
C31	2383441B32	47 uF ±20%; 20 V 800 uF -10 +70%; 30 V
C32	2382077C29	800 uF -10 +70%; 30 V
C33	2383397D06	800 uF -10 +70%; 30 V 0.22 uF +20%; 35 V 15 + 20%; 20 V
C34	2383441B26	15 <u>+</u> 20%; 20 V
C35, 36	2182428B18	.02 uF
		DIODE: See Note I
CR1, 2, 3	4883654H01	Silicon
CR1, 2, 3 CR4 thru 8	4882466H13	Silicon
CR11, 12, 13	4882466H13	Silicon
C2(11, 12, 13	1	
		JACK:
	0905382E01	Connector
31	0703302201	Connector
		RELAY:
K1	8005384E01	2 pole Form C
K2	8005385E01	2-pole Form C 1-pole Form A
K2	103000001	1-pole Form A
		TRANSISTOR, See Note I
	40000/0573	TRANSISTOR: See Note I
Q1	4800869571 4800869706	PNP; type M9571
Q2 thru 5		NPN; type M9700
Q6, 7	4800869570	PNP; type M9571 NPN; type M9706 NPN; type M9700 NPN; type M9700
Q8	4800869706	NPN; type M9700
Q9	4800869806	NPN; type M9806
	1	presentation no 1 110m
		RESISTOR, Fixed: n ±10%
		1/4 W unless stated
R1 thru 12	0600124C97	
R13	0600124A73	10k +5%
R14	0600124B06	220k +5%
R15	0600124A73	220k ±5% 10k ±5% 220k ±5%
R16	0600124B06	220k <u>+</u> 5%
R17	0600124C65	4. /k
R18	0600124C83	27k
R19	0600124A99	120k <u>+</u> 5% 390k <u>+</u> 5%
R20	0600124B12	390k <u>+</u> 5%
R21, 22, 23	0600124C97	100k
R24	0600124C25	100
R25	0600124C97	100k
R26	0600124C83	27k
R27	0600124B06	220k +5%
R28	0600124C83	27k
R29	0600124A93	68k ±5%
R30	0600124C83	27k
	0600124C83	560k <u>+</u> 5%
R31	0600124B16 0600124C97	100k
R32, 33	0600124C17	47
R34	0600124C17	100k
R42, 43		100k
R46 thru 61	0600124C97	
R62, 63	0600124A73	10k ±5%
R64	0600124C41	470
R65	0600124C45	680 56k
R66	0600124C91	
R67	0600124C41	470
R68	0600124B06 0682672B99	220k
R69	0682672899	261k <u>+</u> 1%

	4210217A02	STRAP, Cable Harness STRAP, Cable Harness
	0705387E01 0905261D05 0905382E01 0905388E02 1405383E01 2605380E01 1405474E01 4210122A12 4210217A02	SUPPORT CONNECTOR, Wafer CONNECTOR SOCKET, IC INSULATOR, Fuse HEAT SINK SHIELD, Switch CLIP, Retaining
	NONREFERENCE 0105957C50	BOARD and TERMINAL
¥1	4805386E01	CRYSTAL: See Note III Resonator
VR1	4882256C25	DIODE: See Note I Zener, 12 V
U36	5184621K16	Voltage Regulator, type MC78
U29	5182822F52 5184320A12	type MC14527CP
U27 U29	5182822F52 5182822F52	BCD Rate Multiplier, type MC14527CP BCD Rate Multiplier,
U25	5182822F52 5182822F52	BCD Rate Multiplier, type MC14527CP BCD Rate Multiplier,
U24	5182822F10	Dual Timer, type NE556A Dual D-Type Flip-Flop, type MC14013CP
U22, 26, 28, 30	5184320A85	Factory Programmed Read-C Memory (See Note II) Dual Timer, type NE556A
U21	5182822F52	BCD Rate Multiplier, type MC14527CP
U20	5182822,F08	Quad 2-Input NAND Gate, type MC14011CP
U18 U19	5182822F47 5182822F11	MC14028CP Dual 4-Bit Static Shift Register type MC14015CP
U17	5182822F10 5182822F47	Dual D-type Flip-Flop, type MC14013CP
U16	5182822F34	Dual Binary Up Counter, type MC14520CP
U15	5182822F40	Hex Buffer (Inverting), type MC14049CP
U14	5184320A85	Dual Timer, type NE556A
U13	5182822F03	Quad 2-Input NOR Gate, type MC14001CP
U12	5182822F08	type MC14002CP Quad 2-Input NAND Gate, type MC14011CP
Ull	5182822F25	type MC14507CP Dual 4-Input NOR Gate,
U10	5182822F18	type MC14519CP Quad Exclusive OR Gate,
U9	5182822F28	type MC14011CP 4-Bit and/or Select,
U8	5182822F08	type MC14570CP Quad 2-Input NAND Gate.
U7	5182822F44	type MC14013CP Quad 2-Input OR Gate,
U3 thru 6	5182822F10	type MC14532CP Dual D-Type Flip-Flop,
U1	5182822 F43	Quad 2-Input AND Gate, type MC14571CP 8-Bit Priority Encoder,
S1 U1	4005381E01 5182822 F43	INTEGRATED CIRCUIT:
		SWITCH:
R85 R86	0600124C75 0600125A41	pot, 50k 12k 470 ±5%; 1/2 W
R83 R84	0600124C65 1883083G26	4.7k
R76 R77 thru 82	0682672B99 0600124A73	261k ±1% 10k +5%
R72, 73 R74 R75	0683175C64 0683175C76	51.1k ±1% 60.4k ±1% 90.9k ±1%
	0683175C60	60.4k ±1%

NLN4487A Moden 100 NLN4480A Moden 36

PLF-1179-0 NLN4483A Alert Central REFERENCE MOTOROLA DESCRIPTION SYMBOL PART NO. Pl 0905259D01 Board Connector SWITCH: 12-Position Keyboard S2 4005378E01

NONREFERENCI	ED ITEMS
NONREFERENCE 0200877296 0210101A25 0210101A44 0300007362 03105349E01 0x 1305349E02 0jr 1305349E02 0jr 1305349E03 2905260D01 3805352E01 3805352E04 3805352E04 3805352E06 3805352E06 3805352E07 3805352E08 3805352E09 3805352E09 3805352E09 3805352E09 3805352E09	NUT, Elastic Stop; 2-56 NUT, Spring Type U NUT, Steel; Plain SCREW, 6-36 x 1/2 LOCKWASHER #6 ESCUTCHEON, Keyboard (NLN4487A) ESCUTCHEON, Keyboard (NLN4480A) ESCUTCHEON, Keyboard (NLN4480A) TERMINAL KEY TOP, #1 KEY TOP, #2 KEY TOP, #3 KEY TOP, #4 KEY TOP, #5 KEY TOP, #6 KEY TOP, #6 KEY TOP, #7 KEY TOP, #8 KEY TOP, #8 KEY TOP, #8 KEY TOP, #8 KEY TOP, #9 KEY TOP, #9 KEY TOP, #0 KEY TOP, Letter T KEY TOP, Letter P
3805352E13 4210217A02 4282143C01	KEY TOP, Blank STRAP, Cable Harness CLAMP, Cable
4282143C01 5505475E01 6105350E01	CLAMP, Cable KEY, Polarizing WINDOW

Display Readout Kits:
NLN4488A Moden 100
NLN4481A Moden 36
NLN4515A Alast Control

NLN4515A Alert Central		PLF-1180-0	
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION	
CR9, 10	4805389E01	DIODE: See Note I LED, Indicator	
R35 thru 41 R44, 45	0600124C35	RESISTOR, Fixed: A 270 ±10%; 1/4 W	
U32	5182822F28 5182822F06	INTEGRATED CIRCUIT: 4-Bit AND/OR Select Gate; type MC14519CP	
U34, 35	4883477K01	BCD to 7-Segment Latch/ Decoder/Driver; type MC14511CP 7-Segment Diode Array	
	NONREFERENC	ED ITEM .	
8405307E01 CIRCUIT BOARD, LED Disp.			

NOTES:

- I. For optimum performance, order replacement diodes and transistors by Motorola part number
- II. When ordering ROM's, specify ROM Kit number: NLN1442A for "Moden" 100 and NLN1435A for "Moden" 36 and Alert Central. Also, specify tone group to be programmed.
- III. When ordering crystal units, specify operating frequency, crystal frequency, and part number (type).

NLN4484A Subaudible Option PLF-1176-0 REFERENCE MOTOROLA DESCRIPTION PART NO. SYMBOL RESISTOR, Fixed: n 100k ±5%; 1/4 W R77 thru 80 0600124A97

NLN4485A Ton	e-Only Battery Sa	ver Option PLF-1177-O
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R19 R20 R27	0600124B12 0600124B16 0600124A93	RESISTOR, Fixed: \(\) 390k +5%; 1/4 W 560k +5%; 1/4 W 68k +5%; 1/4 W

Base and Transformer Kits: NLN4479A 115 V (Standard)

	NLN4535A 23	0 V (Optional)	PLF-1181-0		
	REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION		
	F1	6500139681 or 6500139680	FUSE: 1/8-Amp., 125 V (NLN4479A) 1/16-Amp., 250 V (NLN4535A)		
	or 6500139680 T1 2505379E01 or 2505379E02 W1 3005284A02 NONREFERENCE	TRANSFORMER: Power (NLN4479A) Power (NLN4535A)			
ı	W1	3005284A02	AC CORD & PLUG: 3-Conductor		
		NONREFERENC	ED ITEMS		
		0200001362 0300007229 0400001719 0400007666 1505348E01 3100120365 4210217A02 4210217A02 4210283A20 4282387D05	NUT, 6-32 x 1/4" x 3/32" SCREW, 6-32 x 3/8 WASHER, Flat LOCKWASHER #6 COVER, Bottom STRIP, Terminal STRAP, Cable Harness CLIP, Cable (Nylon) CLAMP, Cable		

NLN4607A Tone-Only, Fast Timing, Option PLF-1182-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R19 R20 R27	0600124A89 0600124B16 0600124A93	RESISTOR, Fixed: \$\times \pm 110\%\$ 47k \pm 5\%; 1/4 W 560k \pm 5\%; 1/4 W 68k +5\%; 1/4 W

APPENDIX A GLOSSARY

CODE TYPE - pager coding method requiring a prefix letter for each code.

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APPENDIX B BASIC LOGIC CIRCUITS

1. GENERAL

Symbolic logic provides a simplified means of presenting a series of events which are controlled by two-state devices. Most logical operations performed by the terminal are accomplished through the use of TTL (transistortransistor logic) integrated circuits. TTL logic is two-state: high and low where "high" is defined as 5 volts or high impedance and "low" is defined as ground or low impedance. Generally, an active signal is defined as a high signal. The simplest circuit used in the terminal is the inverter circuit which is shown symbolically in Figure 1. The inverter circuit element produces an output which is the inverse of the input; i.e., a logic "high" at the input pin becomes a logic "low" at the output pin and vice versa. A 1 indicates a "high" signal and a 0 indicates a "low" signal.

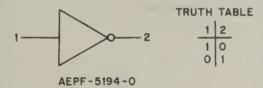


Figure 1. Inverter Circuit

2. GATES

The most basic logic operations involving two or more signals are performed by gating circuits, of which there are several types. Each gate has two or more inputs which correspond to two or more active or inactive input signals. The output can be determined by consulting a "truth table" which lists all combinations of input signals and the resulting output for each combination. The logic symbols and truth tables are shown in Figure 2.

Figure 2. AND/OR Gates

The presence of a circle on a logic symbol indicates the signal is inverted at the circle (a "high" would be changed to a "low" and a "low" would be inverted to a "high"). A circle on the output of an AND gate changes it to a NAND gate. A circle on the output of an OR gate changes it to a NOR gate. A circle on an exclusive-OR gate changes it to an exclusive-NOR gate. These logic symbols and their truth tables are shown in Figure 3. Note that the truth tables are the same as the corresponding tables in Figure 2 except column 3 has the 0 changed to a 1 and the 1 changed to a 0.

Figure 3. NAND/NOR Gates

Sometimes an active signal may be defined as a "low". This signal may be converted to the more conventional "high" by inverting the signal at the input of the logic symbol. Thus a circle on the input of a logic symbol indicates that the signal, when active, is a "low". The symbols are corresponding truth tables are shown in Figure 4. Note that the negative-OR gate and the truth table for the negative-AND gate is the same as that of the NOR gate.

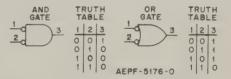


Figure 4. Inverted Inputs

3. RS TYPE FLIP-FLOPS

A simple RS flip-flop, composed of two NAND gates, is shown in Figure 5. The S denotes a "set" input and the R denotes a "reset" input.

The "set" input switches the circuit to the logically active state. The "reset" input returns the circuit to the "non-active" state. The bars above the letters indicate that these inputs are "active low"; that is, these inputs trigger their intended functions when they are at the low logic level (.2 V max.). The outputs are shown in the "set" condition (Q low, Q high). Assume that a low R input has occurred and the circuit is in the reset condition (Q high, Q low). The next low S pulse will deactivate gate B producing a high Q output. The O output will now activate gate A producing a low Q. The circuit will remain in this condition until the next "reset" pulse is applied at the R input. The flip-flop is "storing" an input. When a low pulse is applied at R, gate A is deactivated and Q goes high. The high Q level activates gate B at this time and the Q output goes low. The circuit is now in the "reset" condition and ready for the next input.

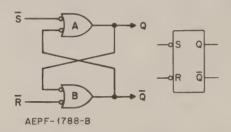


Figure 5. RS Flip-Flop

A fairly simple extension of the RS type flip-flop is produced by the addition of a 2-input NAND gate to both the "set" and "reset" inputs. This addition is shown in Figure 6. One of the inputs to each NAND gate is tied to a common clock or trigger line. A change of state is therefore inhibited until a positive-going clock pulse is applied. This effectively synchronizes the operation of the flip-flop to the clock rate. The truth table is the same as that for the RS flip-flop. For example, assume that a low R input has occurred and the circuit is in the reset

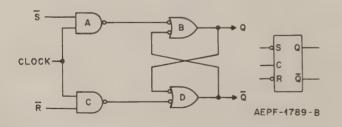


Figure 6. 2-Input RS Flip-Flop

condition (\overline{Q} high, Q low). The next high \overline{S} pulse will enable gate A so that when the positive-going clock pulse arrives, NAND gate B will deactivate and result in a high Q output. The Q output will now activate gate D, producing a low \overline{Q} output.

4. D-TYPE FLIP-FLOP

Another clocked flip-flop is the D-type which provides for separate direct set and reset inputs, in addition to the data (D) input and the clock input; see Figure 7. In this circuit, the single-ended D input is connected directly to the gate input (gate A). An inverter is provided between the input line (D) and the reset (R) input. This ensures that the set and reset inputs cannot be high at the same time. The flip-flop employs a 3-input NAND gate on each side of the circuit (gates B and E) to provide for the direct set and reset inputs. Thus, the flip-flop can be set or reset directly, irrespective of the clock input. During the clock transition, the state of the D input is transferred to the Q output, as shown in the truth table. D_N refers to the time at which clock pulse N occurs, while Q_{N+1} refers to the time at which the following clock pulse occurs.

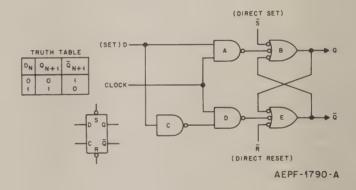


Figure 7. D-Type Flip-Flop

5. J-K TYPE FLIP-FLOP

Still another type of flip-flop used in the terminal is the J-K flip-flop. This type also has direct set and direct reset inputs as described for the D-type flip-flop. However, it has two data inputs which are the so-called J and K inputs. The logic circuit diagram is given in Figure 8. Here, the J-K flip-flop triggers on

the negative edge of the clock input. Data may be applied to or changed at the clocked inputs at any time during the clock cycle, except during the time interval between the setup and hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data states at the inputs throughout the interval between the setup and hold times is stored in the flip-flop when the clock pulse fails. The flip-flop may be set at any time without regard to the clock state by applying a low level to the S input. In addition, the flip-flop may be reset by using the R input at any time.

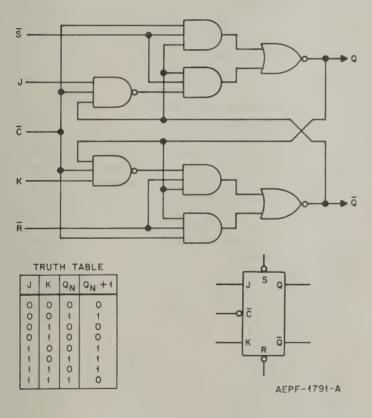


Figure 8. J-K Flip-Flop

6. RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

The retriggerable monostable multivibrator produces an accurately timed output pulse from either edge of an input pulse. The output pulse width may be varied from 40 nanoseconds to 40 seconds by using appropriate external timing components. Referring to Figure 9, inputs A and Bare negative-edge triggered and will trigger the multivibrator into the active state when either or both go low while both C and D are high. C and D inputs will trigger the multibrator when they both go high while either A or B is low. Triggering occurs at a particular voltage level and is independent of the input pulse transition time. The duration and accuracy of the complementary output pulses (Q and Q) are determined by the external timing components R_x and C_x . Each time the input conditions for triggering are met, the external timing capacitor (C_x) is discharged, starting a new output pulse. The output goes to the high state while Cx is being discharged and remains there until the capacitor recharges through Rx to a threshold determined by an internal comparator. Input pulses applied during the active state again discharge the capacitor, thus adding another full timing cycle to the output pulse width. For applications where retriggering is not required, appropriate feedback from the outputs (shown by the dotted lines) will inhibit trigger pulses arriving during the active timing cvcle.

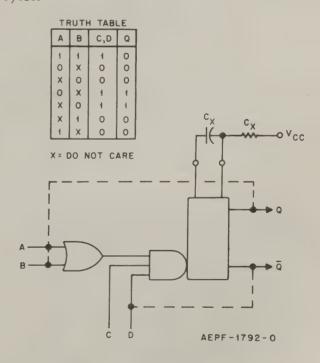
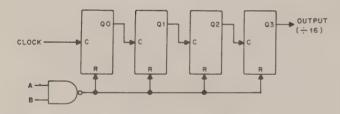


Figure 9. Retriggerable Multivibrator

7. 4-BIT BINARY COUNTER

The 4-bit binary counter consists of four clocked flip-flops connected to provide a divideby-16 function; i. e., the counter counts in straight binary (ripple) fashion. Connections to the counter are made so that the Q output of each flip-flop drives the clock (C) input of the following flip-flop. Thus, each time a flip-flop is reset, the Qoutput falls and triggers the following flip-flop into the set state. The logic diagram given in Figure 10 and the accompanying truth table and timing diagram illustrate the straight binary operation of the counter. When the count reaches 15, all flip-flops are reset by the next clock pulse and the count "rolls over" to zero. A common gated reset input (R) is provided to preset the counter to the zero state (count 0) at any time.

COUNTING SEQUENCE TRUTH TABLE					
COUNT		OUTPUT			
COON	Q3	Q2	Q1	QO	
0	0	0	0	0	ı
1	0	0	0	4	ı
2	0	0	4	0	i
3	0	0	1		i
4	0	1	0	0	l
5	0	1	0	4	ı
6	0	1	4	0	ı
7	0	1	1	1	
8	1	0	0	0	ı
9	1	0	0	0	ı
10	1	0	1	0	ı
- 11	1	0	1		ı
12	1	1	0	0	ı
13	1	1	0	0	ı
14	1	1	1	0	ı
15	1	f	1	1	



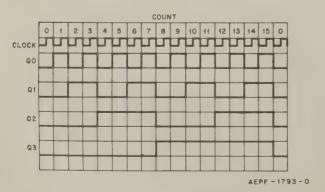


Figure 10. 4-Bit Counter

8. PRESETTABLE 4-BIT BINARY COUNTER

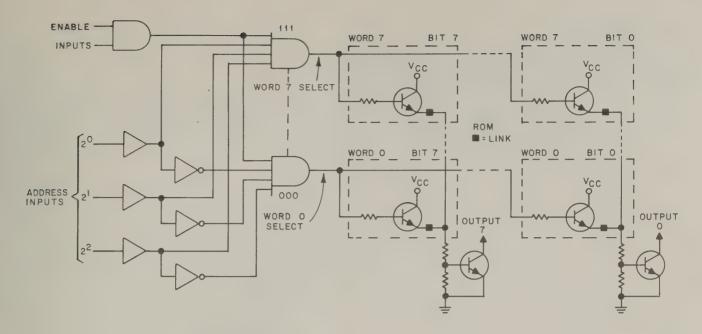
The presettable 4-bit binary counter consists of four clocked J-K flip-flops connected to provide a divide-by-16 function; i.e., the counter counts in a straight binary fashion as described for the 4-bit binary counter in Figure 10. However, this counter also contains additional parallel inputs for presetting data into the counter and parallel outputs for full counting flexibility. Parallel information may be preset only while the parallel enable signal at pin 9 is in the logic 0 state.

Four of these counters are used in the 16-bit tone synthesizer of the terminal output unit. Here, a 16-bit preset word is applied to the parallel inputs (2⁰...2³) of each of the four counters to shorten the time required to reach the full count. In operation, a stable oscillator clocks the counter and when the full count is reached, the counter logic produces a change of state in the output and begins the count at the preset value. The output from the overall counter, therefore, is a continuous squarewave at a fraction of the oscillator frequency. The counting sequence truth table and timing diagram for the presettable counter are the same as that given in Figure 10 for the 4-bit binary counter.

9. ONE-OF-EIGHT DECODER

The one-of-eight decoder consists of a 64-bit read-only memory (ROM), capable of holding eight 8-bit words, and appropriate address decoding and readout control gating logic. A 3-bit binary input address selects the desired word for the 8-bit output. A separate 2-input AND gate is also provided for enabling the network of address decoding gates. The truth table shown in Figure 11 indicates the contents of each 8-bit word and its associated 3-bit address. The ROM consists essentially of an array of 64 emitter followers, arranged in an 8-by-8 matrix, and a set of eight readout transistors; see Figure 11.

In operation, when a particular address has been decoded, a full column of eight transistors will be turned on. The positive voltage then present at each emitter will turn on the associated readout transistor if the metalization link is in place; i.e., a logic 1 is transferred to the emitter of each readout transistor where the link is in place, but a logic 0 is transferred where the link is removed. Thus, the ROM can be programmed once to readout the words shown in the truth table and this will remain fixed unless the metalization links are changed.



TRUTH TABLE

ADD	ADDRESS IN			OUTPUT						
22	21	20	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1	1	1	1
0	0	1	- 1	0	1	1	1	1	-1	1
0	-1	0	1	4	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1_
1	0	0	1	1	1	1	0	1	1	i
1	0	1	-1	1	1	1	1	0	1	1
1	-1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

AEPF-1794-0

Figure 11. One-of-Eight Decoder



APPENDIX C INTEGRATED CIRCUIT PACKAGES

Data sheets of all the integrated circuit packages used in the paging encoder are present in this appendix. The packages are grouped according to manufacturer and then illustrated in sequence by type number. These numbers correspond to those shown on the schematic diagram.

TYPE]	PAGE
Motorola MC14001CP, "NOR" Gate		C-2
Motorola MC14002CP, "NOR" Gate		C-3
Motorola MC14011CP, "NAND" Gate		C-4
Motorola MC14013CP, Flip-Flop		C-5
Motorola MC14015CP, Shift Register		C-6
Motorola MC14028CP, Decoder		C-7
Motorola MC14049CP, Buffers		C-8
Motorola MC14071CP, "OR" Gate		C-9
Motorola MC14081CP, "AND" Gate		C-10
Motorola MC14507CP, Exclusive "OR" Gate		C-11
Motorola MC14511CP, Latch/Decoder/Driver		C-12
Motorola MC14519CP, Selector		C-13
Motorola MC14520CP, Counter		C-14
Motorola MC14527CP, Multiplier		C-15
Motorola MC14532CP, Priority Encoder		C-16
Motorola MC1458CP1, Operational Amplifiers		C-17
Motorola MC7800CP, Voltage Regulator		C-18
Harris HM1-0186, Commercial Diode Matrix (8x6)		C-19
Signetics 556, Dual Timer		C-21

"NOR" GATE

MC14001AL MC14001CL MC14001CP

QUAD 2-INPUT "NOR" GATE

The MC14001 quad 2-Input NOR gate is constructed with MOS P-channel and N-channel enhnacement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of VDD typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14001AL)
 = 3.0 Vdc to 16 Vdc (MC14001CL/CP)
- Single Supply Operation Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4001A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NOR" GATE



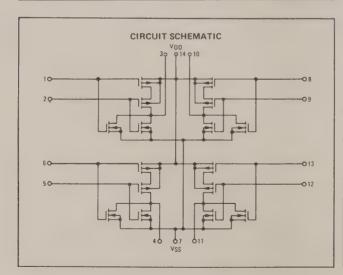


L SUFFIX CERAMIC PACKAGE CASE 632

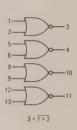
P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to VSS, Pin 7)

Ratio	ng	Symbol	Value	Unit
DC Supply Voltage	MC14001AL MC14001CL/CP	V _{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		Vin	V _{DD} to -0.5	Vdc
DC Current Drain per Pin		1	10	mAdc
Operating Temperature R	ange - MC14001AL - MC14001CL/CP	TA	-55 to +125 -40 to +85	°C
Storage Temperature Ran	nge	T _{stg}	-65 to +150	°C



LOGIC DIAGRAM POSITIVE LOGIC



VDD = Pin 14 VSS = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

"NOR" GATE

MC14002AL MC14002CL MC14002CP

DUAL 4-INPUT "NOR" GATE

The MC14002 dual 4-input NOR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14002AL)
 - = 3.0 Vdc to 16 Vdc (MC14002CL/CP)
- Single Supply Operation Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4002A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "NOR" GATE



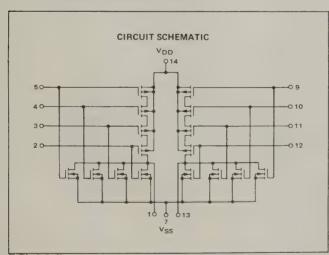


L SUFFIX CERAMIC PACKAGE CASE 632

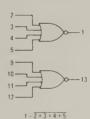
PSUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14002AL MC14002CL/CP	V _{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		Vin	V _{DD} to -0.5	Vdc
DC Current Drain per Pin		ı	10	mAdc
Operating Temperature Ra	nge - MC14002AL - MC14002CL/CP	TA	-55 to +125 -40 to +85	°C
Storage Temperature Rang	е	T _{stg}	-65 to +150	°C



LOGIC DIAGRAM POSITIVE LOGIC



V_{DD} = Pin 14 V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

MC14011AL MC14011CL MC14011CP

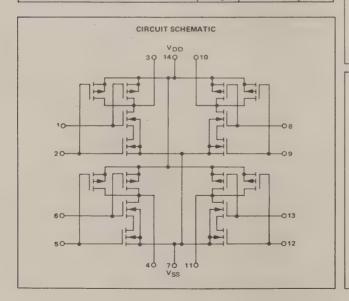
QUAD 2-INPUT "NAND" GATE

The MC14011 quad 2-input NAND gate finds primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14011AL)
 3.0 Vdc to 16 Vdc (MC14011CL/CP)
- Single Supply Operation Positive or Negative
- High Fanout -> 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4011A

MAXIMUM RATINGS (Voltages referenced to VSS, Pin 8.)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14011AL MC14011CL/CP	V _{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		Vin	V _{DD} to -0.5	Vdc
DC Current Drain per Pin		ı	10	mAdc
Operating Temperature Range	MC14011AL MC14011CL/CP	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range		T _{stq}	-65 to +150	°C



McMOS

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NAND" GATE



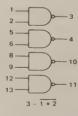
CERAMIC PACKAGE CASE 632

PSUFFIX
PLASTIC PACKAGE
CASE 646

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

LOGIC DIAGRAM POSITIVE LOGIC



V_{DD} = Pin 14 V_{SS} = Pin 7

FLIP-FLOP

MC14013AL MC14013CL MC14013CP

DUAL TYPE D FLIP-FLOP

The MC14013 dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and $\overline{\Omega}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Static Operation
- Quiescent Power Dissipation = 5.0 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of VDD typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14013AL) = 3.0 Vdc to 16 Vdc (MC14013CL/CP)
- Single Supply Operation
- Toggle Rate = 10 MHz
- Logic Edge-Clocked Flip-Flop Design —
 Logic state is retained indefinitely with clock level either high
 or low; information is transferred to the output only on the
 positive-going edge of the clock pulse.
- Pin-for-Pin Replacement for CD4013A

MAXIMUM RATINGS (Voltages referenced to VSS, Pin 7)

Rating	Symbol	Value	Unit
DC Supply Voltage MC14013AL MC14013CL/CP	VDD	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	Vin	V _{DD} to -0.5	Vdc
DC Current Drain per Pin		10	mAdc
Operating Temperature Range - MC14013AL - MC14013CL/CP	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

TRUTH TABLE

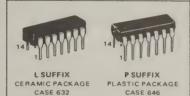
	PUTS	OUT				
	ā	Q	SET	RESET	DATA	CLOCK [†]
	1	0	0	0	0	
	0	1	0	0	1	
No. Chang	ā	Q	0	0	×	7
	1	0	0	1	×	×
	0	1	1	0	×	×
	1	1	1	1	V	Y

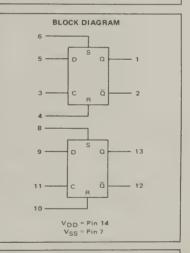
X = Don't Care † = Level Change

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL TYPE D FLIP-FLOP





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that $V_{\rm in}$ and $V_{\rm OUL}$ is constrained to the range $V_{\rm SS} \leqslant (V_{\rm in})$ or $V_{\rm OUL} \leqslant V_{\rm DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or V_{DD}).

MC14015AL MC14015CL MC14015CP

DUAL 4-BIT STATIC SHIFT REGISTER

The MC14015 dual 4-bit static shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of two identical, independent 4-stage serial-input/parallel-output registers. Each register has independent Clock and Reset inputs with a single serial Data input. The register stages are type D master-slave flip-flops. Data is shifted from one stage to the next during the positive-going clock transition. Each register can be cleared when a high level is applied on the Reset line. These complementary MOS shift registers find primary use in buffer storage and serial-to-parallel conversion where low power dissipation and/or noise immunity is desired.

- Quiescent Power Dissipation = 2.5 μW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14015AL) = 3.0 Vdc to 16 Vdc (MC14015CL/CP)
- Single Supply Operation Positive or Negative
- High Fanout >50
- Input Impedance = 1012 ohms typical
- Low Input Capacitance 5.0 pF typical
- Logic Swing Independent of Fanout
- Toggle Rate = 6.0 MHz @ 10 Vdc
- Logic Edge-Clocked Flip-Flop Design —
 Logic state is retained indefinitely with clock level either high
 or low; information is transferred to the output only on the
 positive-going edge of the clock pulse.

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rati	ng	Symbol	Value	Unit
DC Supply Voltage	MC14014A L MC14015C L/CP	V _{DD} +18 to -0.5 +16 to -0.5		Vdc
Input Voltage, All Input	S	Vin	V _{DD} to -0.5	Vdc
DC Current Drain per Pi	n	1	10	mAdic
Operating Temperature F	Range – MC14015A L – MC14015C L/CP	TA	-55 to +125 -40 to +85	°C
Storage Temperature Ra	nge	T _{stg}	-65 to +150	°C

TRUTH TABLES

CLOCKED OPERATION (SYNCHRONOUS)

ı	D	Qn	Q _{n+1}
ı	0	0	0
į	0	1	0
i	1	0	1
ı	1	1	1
			-

Q_{n+1} = D_n, R = 0

DIRECT OPERATION (ASYNCHRONOUS)



McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-BIT STATIC SHIFT REGISTER

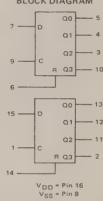




L SUFFIX
CERAMIC PACKAGE,
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to evoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

DECODER

MC14028AL MC14028CL MC14028CP

BCD-TO-DECIMAL DECODER BINARY-TO-OCTAL DECODER

The MC14028 decoder is constructed so that an 8421 BCD code on the four inputs provides a decimal (one-of-ten) decoded output, while a 3-bit binary input provides a decoded octal (one-of-eight) code output with D forced to a logic "0". Expanded decoding such as binary-to-hexadecimal (one-of-16), etc., can be achieved by using other MC14028 devices. The part is useful for code conversion, address decoding, memory selection control, demultiplexing, or readout decoding.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- High Fanout -> 50
- Buffered Outputs Compatible with HTL and Low-Power TTL
- Positive Logic Design
- Low Power Dissipation of 25 nW/package typical @ V_{DD} = 5.0 V
- Low Outputs on All Illegal Input Combinations
- Pin-for-Pin Replacement for CD4028A

MAXIMUM RATINGS (Voltages referenced to VSS, Pin 8)

Ratin	Symbol	Value	Unit	
DC Supply Voltage	MC14028AL MC14028CL/CP	V _{DD}	+18 to -0 5 +16 to -0 5	Vdc
Input Voltage, All Inputs		V _{in}	V _{DD} to -05	Vdc
DC Current Drain per Pir		1	10	mAdc
Operating Temperature F	TA	-55 to +125 -40 to +85	°C	
Storage Temperature Ran	nge	T _{stg}	-65 to +150	°C

BLOCK DIAGRAM _0 3 10 0-00 Q 1 ---0 14 Q2 **-**0 2 3-Bit Octal Binary 13.0-03 -0 15 Decoded 8421 Decimal Inputs **--**0 1 Q4 Outputs BCD Decoded -06 Inputs 05 Outputs 12 0-Q6 -0 7 -04 07 Q8 ---09 09 V_{DD} = Pin 16 V_{SS} = Pin 8

McMOS

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-DECIMAL DECODER BINARY-TO-OCTAL DECODER





L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

TRUTH TABLE

	INF	TU					С	UT	PU	T			
D	С	В	Α	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	00
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	3	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

BUFFERS

MC14049AL MC14049CL MC14049CP MC14050AL MC14050CL MC14050CP

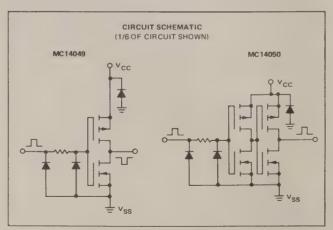
HEX BUFFERS

The MC14049 hex inverter/buffer and MC14050 noninverting hex buffer are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic-level conversion using only one supply voltage, VCC. The input-signal high level (V1H) can exceed the VCC supply voltage for logic-level conversions. Two TTL/DTL loads can be driven when the devices are used as CMOS-to-TTL/DTL converters (VCC = 5.0 V, VOL \leq 0.4 V, IOL \geq 3.2 mA). Note that pin 16 is not connected internally on these devices; consequently connections to this terminal will not affect circuit operation.

- Direct Drive of Two TTL/DTL Loads
- High Source and Sink Currents
- High-to-Low or Low-to-High Level Converter
- Quiescent Power Dissipation = 5 nW/package typical @ 5 Vdc
- Single-Supply, Pin-for-Pin Replacements for Types MC14009 and MC14010 Respectively

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit	
DC Supply Voltage	AL Version	Vcc	+18 to -0.5	Vdc
_	CL,CP Version		+16 to -0.5	
Input Voltage, All Inputs		Vin	+18 to -0.5	Vdc
DC Current per Input Pin		lin	10	mAdc
DC Current per Output Pin		lout	45	mAdc
Operating Temperature Range	AL Version	TA	-55 to +125	°C
	CL,CP Version		-40 to +85	
Storage Temperature Range		T _{stg}	-65 to +150	°C
Maximum Dissipation per Pack	age	PD	See Figure 1	



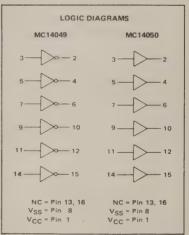
McMOS

(LOW-POWER COMPLEMENTARY MOS)

HEX BUFFERS

Inverting — MC14049AL/CL/CP Noninverting — MC14050AL/CL/CP





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VCC).

"OR" GATE

MC14071AL MC14071CL MC14071CP

QUAD 2-INPUT "OR" GATE

The MC14071 quad 2-input OR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14071AL) = 3.0 Vdc to 16 Vdc (MC14071CL/CP)
- Single Supply Operation Positive or Negative
- High Fanout > 50
- Input Impedance = 10¹² ohms typical
- Logic Swing Independent of Fanout

McMOS

(LOW POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "OR" GATE



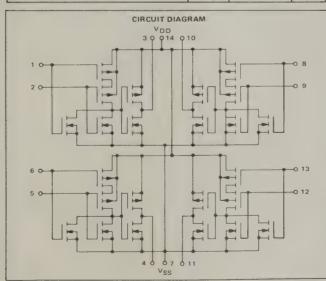


L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to VSS, Pin 7.

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14071AL MC14071CL/CP	V _{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		Vin	V _{DD} to -0.5	Vdc
DC Current Drain per Pin		1	10	mAdc
Operating Temperature Rang	e - MC14071AL - MC14071CL/CP	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range		T _{stg}	-65 to +150	°C



LOGIC DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

"AND" GATE

MC14081AL MC14081CL MC14081CP

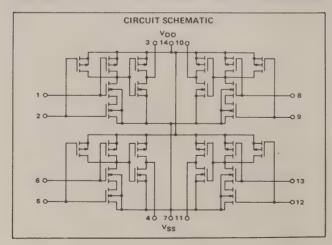
QUAD 2-INPUT "AND" GATE

The MC14081 quad 2-Input AND gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14081AL)
 3.0 Vdc to 16 Vdc (MC14081CL/CP)
- Single Supply Operation Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14081AL MC14081CL/CP	VDD	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		Vin	V _{DD} to -0.5	Vdc
DC Current Drain per Pin		1	10	mAdc
Operating Temperature Range	ge -MC14081AL -MC14081CL/CP	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range		T _{stg}	-65 to +150	°C



McMOS

(LOW-POWER COMPLEMENTARY MOS)
QUAD 2-INPUT "AND" GATE



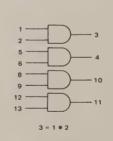


CERAMIC PACKAGE CASE 632 P SUFFIX
PLASTIC PACKAGE
CASE 646

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either v_{SS} or $v_{DD}). \\$

LOGIC DIAGRAM



V_{DD} = Pin 14 V_{SS} = Pin 7

EXCLUSIVE "OR" GATE

MC14507AL MC14507CL MC14507CP

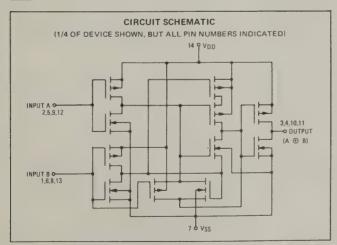
QUAD EXCLUSIVE "OR" GATE

The MC14507AL/CL quad exclusive OR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14507AL)
 3.0 Vdc to 16 Vdc (MC14507CL/CP)
- Single Supply Operation Positive or Negative
- High Fanout -> 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-For-Pin Compatible with 4030 Type

MAXIMUM RATINGS (Voltages referenced to VSS, Pin 7)

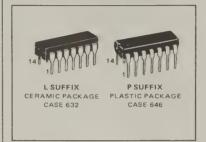
Rati	ng	Symbol	Value	Unit	
DC Supply Voltage	-MC14507AL -MC14507CL/CP	V _{DD}	+18 to -0.5 +16 to -0.5	Vdc	
Input Voltage, All Inputs	3	V _{in}	V _{DD} to -0.5	Vdc	
DC Current Drain per Pir	1		10	mAdc	
Operating Temperature R	ange -MC14507AL -MC14507CL/CP	Тд	-55 to +125 -40 to +85	°C	
Storage Temperature Rai	nge	T _{stg}	-65 to +150	°C	



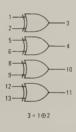
McMOS

(LOW-POWER COMPLEMENTARY MOS)

QUAD EXCLUSIVE "OR" GATE



LOGIC DIAGRAM POSITIVE LOGIC



V_{DD} = Pin 14 V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or $V_{DD}). \label{eq:vss}$

LATCH/DECODER/DRIVER

MC14511AL MC14511CL MC14511CP

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

The MC14511 BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test (\overline{LT}), blanking ($\overline{B1}$), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High-Current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage - MC14511AL - MC14511CL/CP	V _{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	Vin	V _{DD} to -0.5	Vdc
Operating Temperature Range – MC14511AL – MC14511CL/CP	ТА	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C
Maximum Continuous Output Drive Current (Source) per Output	¹ OHmax	25	mA
Maximum Continuous Output Power (Source) per Output ‡	POHmax	50	mW

^{\$} POHmax = IOH (VDD - VOH)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occure if V_{in} and V_{out} is not constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

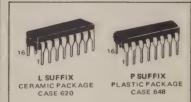
Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

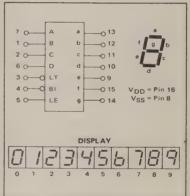
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

McMOS

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER





<u> </u>														
TRUTH TABLE														
	INPUTS										Oi	TP	UTS	5
LE	BI	LŤ	D	С	В	Α	a	b	С	d	e	f	g	DISPLAY
×	×	0	×	×	×	×	7	1	1	1	1	1	1	8
×	0	1	X	×	×	X	0	0	0	0	0	0	0	Blank
0	1	7	0	0	0	0	1	1	1	- 1	1	1	0	0
0		1	0	0	0	9	0	1	1	o	0	o	o	1
0	1	1	0	0	- 1	0	1	2	0	1	1	0	1	2
0	1	1	0	0	1	3	1	- 1	1	1	o	0	- 1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	7	4
0	- 1	1	0	1	0	1	1	0	1	1	0	1	9	5
0	- 1	1	0	1	1	0	0	0	1	- 1	1	9	1	6
0	1	1	0	1	1	1	1	1	3	0	ò	ė	0	7
0	1	1	1	0	0	0	1	1	9	1	7	1	2	8
0	1	1	1	0	0	1	3	1	1	0	ò	1	i	9
0	1	1	- 1	0	1	0	0	ò	ò	0	0	ò	0	Blank
0	1	1	1	0	1	2	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	o	a	0	Blank
0	1 :	9	1	1	1	0	0	0	0	o	0	0	0	Black
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	7	1	×	×	Х	X	_	_	_	0	_	-	_	

X = Don't Care
*Depends upon the BCD code previously applied

COUNTERS

MC14518AL MC14518CL MC14518CP MC14520AL MC14520CL MC14520CP

DUAL UP COUNTERS

The MC14518 dual BCD counter and the MC14520 dual binary counter are constructed with MOS P-channel and Nchannel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518 will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity

- Quiescent Power Dissipation = 1.0 μW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14518AL and MC14520AL)
 - = 3.0 Vdc to 16 Vdc (MC14518CL,CP and MC14520CL,CP)
- Low Input Capacitance = 5.0 pF typical
- Internally Synchronous for High Internal and External Speeds.
- Logic Edge-Clocked Design Incremented on Positive Transition of Clock or Negative Transition on Enable
- 6.0 MHz Counting Rate

MAXIMUM RATINGS (Voltages referenced to Voc Pin 8

Rating	Symbol	Value	Unit	
DC Supply-Voltage -MC14518AL/520AL -MC14518CL,CP/520CL,CP	V _{DD}	+18 to -0.5 +16 to -0.5	Vdc	
Input Voltage, All Inputs	Vin	V _{DD} to -0.5	Vdc	
DC Current Drain Per Pin	I 10		mAdc	
Operating Temperature Range MC14518AL/520AL MC14518CL,CP/520CL,CP	TA	-55 to +125 -40 to +85	°C	
Storage Temperature Range	T _{stg}	-65 to +150	°C	

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
5	1	0	Increment Counter
0	~	0	Increment Counter
~	×	0	No Change
Х		0	No Change
	0	0	No Change
1	~	0	No Change
Х	х	1	Q1 thru Q4 = 0

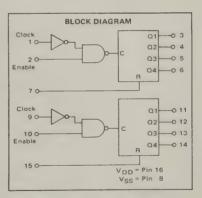
X = Don't Care

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL BCD UP COUNTER (MC14518) **DUAL BINARY UP COUNTER** (MC14520)





This device contains circuitry to protect the This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance num rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le |V_{in} \text{ or } V_{out}| \le V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS}

or VDD)

SELECTOR

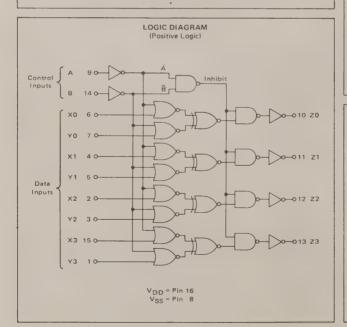
MC14519AL MC14519CL MC14519CP

4-BIT AND/OR SELECTOR or QUAD 2-CHANNEL DATA SELECTOR or QUAD EXCLUSIVE "NOR" GATE

The MC14519 is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

This device exemplifies the design versatility of MCMOS logic structure. This part provides three functions in one package; a 4-Bit AND/OR Selector, a Quad 2-Channel Data Selector, or a Quad Exclusive NOR Gate.

- Quiescent Power Dissipation = 25 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14519AL)
 3.0 Vdc to 16 Vdc (MC14519CL/CP)
- Single Supply Operation Positive or Negative
- High Fanout > 50
- Input Impedance = 1012 ohms typical
- Logic Swing Independent of Fanout
- Plug-In Replacement for CD4019 in Most Applications



McMOS

(LOW-POWER COMPLEMENTARY MOS)

4-BIT AND/OR SELECTOR





L SUFFIX CERAMIC PACKAGE CASE 620

PSUFFIX
PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

TRUTH TABLE

CONTROL	INPUTS	OUTPUT			
А	В	Zn			
0	0	0			
0	1	Yn			
1	0	Xn			
1	1	× _n ⊚ Y _n			

X_n Y_n means X_n (Exclusive-NOR) Y_n

MC14527AL MC14527CL MC14527CP

BCD RATE MULTIPLIER

The MC14527 BCD rate multiplier (DRM) provides an output pulse rate based upon the BCD input number. For example, if 6 is the BCD input number, there will be six output pulses for every ten input pulses. This part may be used to add, subtract, divide, raise to power, and solve algebraic and differential equations, and can be used to generate trigonometric functions and natural logarithms. Typical applications include digital filters, motor speed control and frequency synthesizers.

- Quiescent Power Dissipation = 0.25 μW/package typical @ 5.0 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14527AL) = 3.0 Vdc to 16 Vdc (MC14527CL/CP)
- Low Input Capacitance 5.0 pF typical
- Internally Synchronous for High Speed
- Output Clocked on the Negative Going Edge of Clock
- Strobe for Inhibiting or Enabling Outputs
- Enable and Cascade Inputs for Cascade Operation of Two or More DRMs
- "9" Output for the Parallel Enable Configuration and DRMs in Cascade
- Complementary Outputs
- Clear and Set to Nine Inputs

MAXIMUM RATINGS (Voltages referenced to VSS, Pin 8)

Rating	Symbol	Value	Unit	
DC Supply Voltage MC14527AL MC14527CL/CP	V _{DD}	+18 to -0.5 +16 to -0.5	Vdc	
Input Voltage, All Inputs	Vin	V _{DD} to -0.5	Vdc	
DC Current Drain per Pin	1	10	mAdc	
Operating Temperature Range-MC14527AL - MC14527CL/CP	TA	-55 to +125 -40 to +85	°C	
Storage Temperature Range	T _{stg}	-65 to +150	°C	

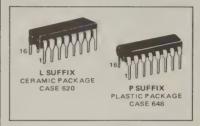
Г											OUT	PUT	
										LOGIC LEVEL			
	INPUTS										ABER (OF PUL	SES
6	С	C B A Clock Pulses E In STROBE CASCADE CLEAR SET							OUT	OUT	Eout	''9''	
-		=	⋍								001	~out	
0	0	0	0	10 10	0	0	0	0	0	0	1	1	1
0	00	A	0	10 10	0	0	0	0	0	2 3	2	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1 1
0	1	H	1	10	0	0	0	0	0	7	7	1	1
1	0	0	o	10	0	ő	ő	Ó	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1.3	0	1	0	10	0	0	0	0	0	8	8		
1	0		1	10	0	0	0				_	-	
1	1	0	0	10	0	0	0	0	0	8	8	1	
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1 1	1	Hill	1	10	0	ő	ő	0	o i	9	9	1	1
×	×	×	×	10	1	ō	0	Ö	0				
×	X	X	X	10	0	1	0	0	0	0	1	1	1
X	X	×	×	10	0	0	1 1	0	0	10	10	1	6
1 1	X	X	X	10	0	0	0	1	0	0	1		ŏ
0 X	X	X	×	10	0	ő	ő	ò	1	ő	í	Ö	1

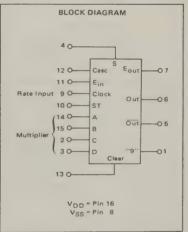
X = Don't Care

McMOS

(LOW-POWER COMPLEMENTARY MOS)

BCD RATE MULTIPLIER





This device contains circuitry to protect This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{out} \log V_{out}$ $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

PRIORITY ENCODER

MC14532AL MC14532CL MC14532CP

8-BIT PRIORITY ENCODER

The MC14532AL/CL/CP is constructed with complementary MOS (CMOS) enhancement mode devices. The primary function of a priority encoder is to provide a binary address for the active input with the highest priority. Eight data inputs (D0 thru D7) and an enable input (Ein) are provided. Five outputs are available, three are address outputs (O0 thru Q2), one group select (GS) and one enable output (Eout).

- Quiescent Power Dissipation = 25 nW/package typical @ 5.0 Vdc
- Noise immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Low Input Capacitance 5.0 pF typical

MAXIMUM RATINGS (Voltage referenced to VSS, Pin 8)

Rating	Symbol	Value	Unit	
DC Supply Voltage MC14532AL MC14532CL/CP	V _{DD}	+18 to -0.5 +16 to -0.5	Vdc	
Input Voltage, All Inputs	Vin	V _{DD} to -0.5	Vdc	
DC Current Drain per Pin	1	10	mAdc	
Operating Temperature Range—MC14532AL —MC14532CL/CP	TA	-55 to +125 -40 to +85	oC	
Storage Temperature Range	T _{stg}	-65 to +150	°C	

TRUTH TABLE

	INPUT									ОИТРИТ				
Ein	D7	D6	D5	D4	D3 :	D2	D1	D0	GS	Q2	Q1	0.0	Eout	
0	X 0	X 0	X 0	X 0	X 0	X 0	X 0	X 0	0	0	0	0	0	
1 1 1	1 0 0 0	X 1 0	X X 1 0	X X X	X X X	X X X	× × ×	X X X	1 1 1 1	1 1 1 1	1 1 0 0	1 0 1 0	0 0 0	
1 1 1 1	0 0 0	0 0	0 0 0	0 0 0	1 0 0	X 1 0	X X 1 0	X X X	1 1 1 1	0 0 0	1 1 0 0	1 0 1 0	0 0 0	

X = Don't Care

McMOS

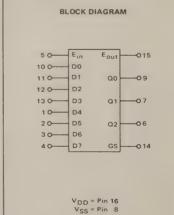
(LOW-POWER COMPLEMENTARY MOS)

8-BIT PRIORITY ENCODER



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $v_{SS} \ {\rm or} \ v_{DD})$



OPERATIONAL AMPLIFIERS

MC1558 MC1458 MC1458C

DUAL MC1741 INTERNALLY COMPENSATED, HIGH PERFORMANCE OPERATIONAL AMPLIFIER

... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

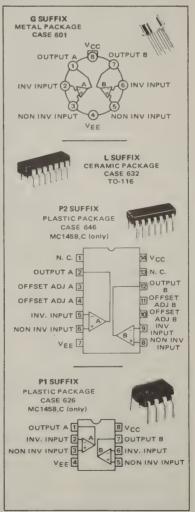
- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

FIGURE 1 — HIGH-IMPEDANCE, HIGH-GAIN INVERTING AMPLIFIER VCC VCC VCC VCC VCC NON-INVERTING INPUT INVERTING INVER

(DUAL MC1741)

DUAL OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



See Packaging Information Section for outline dimensions.

See current MCCF1558/1458 data sheet for flip-chip information.

VOLTAGE REGULATORS

MC7800C **Series**

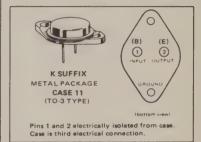
MC7800C SERIES THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC7800C Series of three-terminal positive voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. Available in seven fixed output voltage options from 5.0to-24 volts, these regulators employ internal current limiting, thermal shutdown, and safe area compensation - making them essentially blow-out proof. With adequate heatsinking they can deliver output currents in excess of 1.0 ampere. The last two digits of the part number indicate nominal output voltage.

- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 199-04 (Pin Compatible with the VERSAWATT[†] or TO-220) Or Hermetic TO-3 Type Metal Power Package (Case 11)

THREE-TERMINAL POSITIVE FIXED **VOLTAGE REGULATORS**

SILICON MONOLITHIC INTEGRATED CIRCUITS



SCHEMATIC DIAGRAM 100 \$ 100 € 10 k 2 100 k ₹ 500 ₹ 240 1 200 0.3 2 O Output 3.3 0-25 k Case is ground for Case 11, pin 3 for Case 199-04. 500 € ∃ O Gnd

TYPE NO./VOLTAGE MC7806C 5.0 Volts MC7806C 6.0 Volts

MC7808C 8.0 Volts MC7812C 12 Volts MC7815C 15 Volts

MC7818C 18 Volts MC7824C 24 Volts

See Packaging Information Section for outline dimensions.

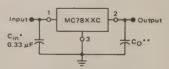
P SUFFIX PLASTIC PACKAGE CASE 199-04

Pin 1 Input (Base) Pin 2 Output (Emitter)

Pin 3 Ground (Collector)

to pin 3.

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

- XX = these two digits of the type number indicate voltage.
- = C_{in} is required if regulator is located an appreciable distance from power supply
- ** = CO is not needed for stability; however, it does improve transient response.

[†]Trademark of Radio Corporation of America.



A DIVISION OF HARRIS-INTERTYPE CORPORATION

HM1-0110 (4x10) HM1-0168 (6x 8)

HM1-0104 (10x 4)

HM1-0186 (8x 6)

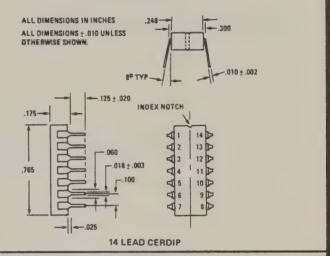
Commercial Diode Matrix

DESCRIPTION

The commercial diode matrices are arrays of passivated silicon diodes, fabricated in dielectrically isolated moats. An epitaxial layer is used as the common cathode connection for all diodes in a row. Column connections to the anode side of the diodes are made through metal interconnect lines via fusible links. By selectively opening the links, diodes can be removed from the circuit to form any desired matrix pattern. This device is available in a 14-lead dual in-line CERDIP package.

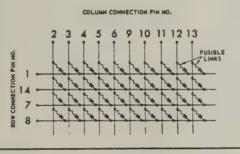
PACKAGE

CODE 1A

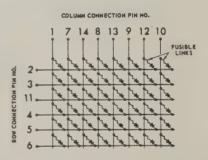


MATRIX PATTERNS

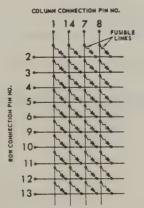
HM1-0110 - 5 (4×10)



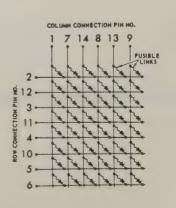
HM1-0168-5 (6×8)



HM1-0104 (10×4)



HM1-0186 (8×6)



ABSOLUTE MAXIMUM RATINGS

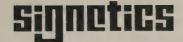
Forward Current 100mA
Surge Current (100 µs Max.) 200mA
Total Circuit Dissipation (Still Air) 450mW
Operating Temperature (Ambient) 0°C to 70°C

ELECTRICAL CHARACTERISTICS AT 25°C

		HM1-0104 (10 x 4) HM1-0168 (6 x 8) HM1-0186 (8 x 6)		HM1-01	10 (4 x 10)			
CHARACTERISTIC		LIMITS		LIMI	TS	CONDITIONS		
		MIN.	MAX.	MIN.	MAX.			
Forward Drop	V _{F20}		1.5V		1.8V	1 _F = 20mA		
Forward Drop	V _{F1}		0.9V		1.0V	I _F = 1mA		
Rev. Breakdown Volt.	BVR	20V		20V		I _R = 100μA		
Rev. Current	1 _R		1µА		1µА	V _R = 15V		
Rev. Rec. Time			100ns		100ns	I _F = 10mA I _R = 10mA to 1mA		
Coupling Capacitance	C _{CP}		8pF		8pF	V _R = 5V f = 1MHz		

NOTE: When ordering a matrix with a custom pattern either obtain copies of Harris patternizing forms from your local sales representative or contact headquarters, Marketing, Melbourne, Florida.

On all orders less than 100 units there will be a one time charge for each special pattern formed by Harris.



LINEAR INTEGRATED CIRCUITS

PIN CONFIGURATION (Top View)

DESCRIPTION

The NE/SE556 Dual Monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 150mA.

FEATURES

- TIMING FROM MICROSECONDS TO HOURS
- REPLACES TWO 555 TIMERS
- OPERATES IN BOTH ASTABLE, MONOSTABLE, TIME DELAY MODES
- HIGH OUTPUT CURRENT
- ADJUSTABLE DUTY CYCLE
- TTL COMPATIBLE
- TEMPERATURE STABILITY OF 0.05% PER °C

APPLICATIONS

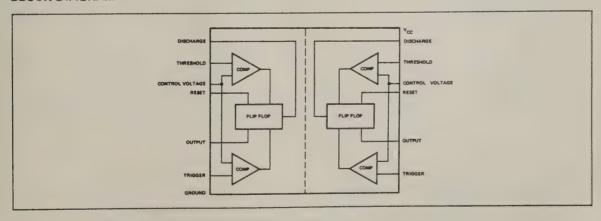
PRECISION TIMING SEQUENTIAL TIMING **PULSE SHAPING PULSE GENERATOR** MISSING PULSE DETECTOR **TONE BURST GENERATOR PULSE WIDTH MODULATION** TIME DELAY GENERATOR FREQUENCY DIVISION INDUSTRIAL CONTROLS **PULSE POSITION MODULATION APPLIANCE TIMING** TRAFFIC LIGHT CONTROL **TOUCH TONE ENCODER**

BLOCK DIAGRAM

A PACKAGE Vcc Discharge Threshold Discharge Control Voltage Threshold Control Voltage Reset Output 9 Output Trigger 8 Trigger Ground

ABSOLUTE MAXIMUM RATINGS

+18V Supply Voltage 600mW **Power Dissipation** 0°C to +70°C Operating Temperature Range NE556 SE556 -55°C to +125°C SE556C -55°C to +125°C -65°C to +150°C Storage Temperature Range Lead Temperature (Soldering, 60 sec) +300°C



ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}C$, $V_{CC} = +5V$ to +15 unless otherwise specified

PARAMETER	TEAT 001171710110		SE 556			NE 556		1100000
	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V _{CC} =5V R _L =∞		3	5		3	6	mA
	V _{CC} = 15V R _L = ∞		10	11		10	14	mA
	Low State, Note 1							
Timing Error (Monostable)	$R_A = 2K\Omega$ to $100K\Omega$							
Initial Accuracy	$C = 0.1 \mu F$ Note 2		0.5	1.5		0.75		%
Drift with Temperature			30	100		50		ppm/°C
Drift with Supply			0.05	0.2		0.1		%/Volt
Voltage	B B - 2KO to 100KO							
Timing Error (Astable)	R_A , $R_B = 2K\Omega$ to $100K\Omega$ $C = 0.1\mu F$ Note 2		1.5			2.25		%
Initial Accuracy Drift with Temperature	C = 0.1µF Note 2	1	90			150		ppm/°C
Drift with Supply			90			150		
Voltage			0.15		1	0.3	1	%/Volt
Threshold Voltage		Į	2/3			2/3		x v _{cc}
Threshold Current	Note 3		30	100		30	100	nA
Trigger Voltage	V _{CC} = 15V	4.8	5	5.2	1	5		V
, , , , , , , , , , , , , , , , , , ,	V _{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current	CC		0.5			0.5		μА
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1	1		0.1		mA
Control Voltage Level	V _{CC} = 15V	9.6	10	10.4	9.0	10	11	V
	V _{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Output Voltage Drip (low)	V _{CC} = 15V							
	ISINK = 10mA		0.1	0.15		0.1	.25	V
	ISINK = 50mA		0.4	0.5		0.4	.75	V
	SINK = 100mA		2.0	2.25		2.0	2.75	V
	ISINK = 200mA		2.5			2.5		
	V _{CC} = 5V		0.1	0.25				V
	ISINK = 8mA		0.1	0.25		.25	.35	· ·
Output Voltage Drop (high)	ISINK = 5mA					.25	.55	
Output Voltage Orop (mgn)	SOURCE = 200mA		12.5			12.5		
	V _{CC} = 15V		1			12.0		
	SOURCE = 100mA							
	V _{CC} = 15V	13.0	13.3		12.75	13.3		V
	V _{CC} = 5V	3.0	3.3		2.75	3.3		V
Rise Time of Output			100			100		nsec
Fall Time of Output			100			100		nsec
Discharge Leakage Current			20	100		20	100	nA
Matching Characteristics								
(Note 4)								
Initial Timing Accuracy			0.05	0.1		0.1	0.2	%
Timing Drift with			±10			±10		ppm/°C
Temperature								
Drift with Supply			0.1	0.2		0.2	0.5	%/Volt
Voltage								

NOTES

- 1. Supply current when output is high is typically 1.0ma less.
- Tested at V_{CC} = 5V and V_{CC} = 15V.
 This will determine the maximum value of R_A + R_B for 15V operation. The maximum total R = 20 meg-ohms.
 Matching characteristics refer to the difference between performance characteristics of each timer section.





